IGBT Structural Design

The methodology for designing the internal structure of the insulated-gate bipolar transistor (IGBT) is systematically presented in this chapter. It is essential that the internal structure be designed to achieve the desired blocking voltage capability. The blocking voltage capability for the IGBT is dictated by the maximum voltage impressed upon the device in its intended application. In typical motor control applications with power delivered from a DC bus, the IGBT can be subjected to spikes in collector voltage that are 50% greater than the DC bus voltage. This margin must be taken into account when designing the blocking voltage capability of the IGBT structure.

All high voltage IGBTs must have reasonable threshold voltage of 4 V. Smaller threshold voltages can lead to inadvertent turn-on of the IGBT due to spikes in voltage on the gate, which are due to the high rate of change in collector voltage during the IGBT switching transients. Larger threshold voltages are not desirable because this requires either an increase in the gate drive voltage or a larger on-state voltage drop. The threshold voltage is determined by a combination of the doping concentration of the \( P \)-base region and the gate oxide thickness.

Various IGBT structures were discussed in the previous chapter. Although two-dimensional effects differ among these structures, it is possible to create one-dimensional models for the IGBT because of a homogenous behavior within the drift region over most of its thickness. These one-dimensional models allow analytical models to be developed that can be used to estimate the optimum thickness and doping concentration of the drift region before resorting to two-dimensional numerical simulations to refine these parameters. One-dimensional analytical models for the injected carrier distribution can also be generated to provide a deeper understanding of the physics of operation of the IGBT structures. The free carrier concentrations determine not only the on-state voltage drop but also the turn-off transients. In this chapter, one-dimensional models are provided for each of the primary IGBT structures discussed in the previous chapter.

As described in this chapter, the parameters of the internal structure can be adjusted to achieve a trade-off between the on-state voltage drop and the turn-off switching losses. In the case of the symmetric blocking IGBT, this is typically done by varying the lifetime in the drift region. In the case of the asymmetric IGBT structure, this can be accomplished by changing the thickness and doping concentration in the buffer layer, as well as by varying the lifetime in the drift region. In the case of the transparent emitter IGBT structure, the trade-off can be performed by varying the doping concentration of the \( P \)-collector region, the doping concentration...
and thickness of the buffer layer, as well as the lifetime in the drift region. The choice between these approaches depends upon the voltage rating of the device, the available process technology, and the know-how developed by each IGBT manufacturer.

### 3.1 Threshold Voltage

The threshold voltage for the IGBT is the minimum gate bias voltage required to observe on-state current flow. Typical IGBT products have a threshold voltage of 4 V with a gate drive voltage of 15 V used for on-state operation. The threshold voltage of high voltage devices is typically larger than for low voltage (e.g., 30-V) power MOSFET products because of the larger voltage transients in IGBT applications that can induce larger spurious voltages on the gate terminal. The design methodology used to achieve a desired threshold voltage is the same for all the IGBT structures discussed in this chapter.

Current flow in the IGBT structure begins to occur when an inversion layer forms in the integrated MOSFET portion, which supplies the electrons that serve as the base drive current for the internal PNP bipolar transistor. The formation of an inversion layer at the surface of the P-base region is induced by the positive gate bias voltage. In IGBT products, the threshold voltage is defined as the gate voltage at which a certain magnitude of collector current is observed. However, from the standpoint of device physics, the threshold voltage is defined as the gate bias at which the transition occurs from weak-inversion to strong-inversion. In the absence of charge in the oxide and any work-function difference between the gate electrode and the semiconductor, the threshold voltage is given by [1]:

$$V_{TH} = \sqrt{\frac{4\varepsilon_S k T N_A}{C_{OX}}} \ln \left(\frac{N_A}{n_i}\right) + 2kT \ln \left(\frac{N_A}{n_i}\right)$$  

(3.1)

where $C_{OX}$ is the specific gate oxide capacitance and $N_A$ is the peak doping concentration of the P-base region. The threshold voltage can be estimated using:

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_S k T N_A \ln \left(\frac{N_A}{n_i}\right)}$$  

(3.2)

where $t_{OX}$ is the gate oxide thickness. Based upon this equation, the threshold voltage increases linearly with increasing gate oxide thickness and approximately as the square root of the doping concentration in the semiconductor. This knowledge can be used to improve the design of IGBT structures as discussed later in the book.

The doping profile of the P-base region in IGBTs produced using the double-diffusion process is illustrated in Fig. 3.1. Both the P-base and $N^+$ emitter regions are formed by using a diffusion process with a surface concentration and junction depth decided by the ion-implant dose and drive-in time. The $n$-type emitter doping compensates the $p$-type base doping near the junction. The net $p$-type doping
concentration in the $P$-base region is indicated by the dashed line in the figure. The highest or peak doping concentration ($N_{AB-Peak}$) in the $P$-base region has a lower value than the surface concentration ($N_{BS}$) of the $P$-base doping profile. The threshold voltage is determined by this doping concentration because of its largest value when compared with the threshold voltage at other portions of the $P$-base doping profile. The simple one-dimensional analytical solution for the threshold voltage pertains to this portion of the $P$-base region with the highest net $p$-type doping level.

For $n$-channel IGBTs, an $n$-type polysilicon gate is utilized because this produces a negative shift in the threshold voltage by about 1 V [1]. This negative shift is desirable because it allows for a higher doping concentration of the $P$-base region to achieve the required threshold voltage. A larger doping concentration for the $P$-base region suppresses the latch-up of the internal thyristor structure within the IGBT structure, making it more rugged in applications. The threshold voltage is also affected by the presence of positive fixed charge in the gate oxide. The fixed charge density is typically $1 \times 10^{11}$ cm$^{-2}$ for IGBT devices due to the high temperature diffusion steps required for the formation of the $P$-base region. This value will be assumed for the computation of the threshold voltages below.

The threshold voltages for silicon $n$-channel IGBTs obtained by using Eqn (3.1) is provided in Fig. 3.2 as a function of the peak doping concentration of the $P$-base
The gate oxide thickness is used as a parametric variable. The design target of a threshold voltage of 4 V is indicated by the dashed line in the figure. During the early days of IGBT development, the gate oxide thickness was maintained at 1000 Å or above to obtain sufficient yield. Modern IGBTs have gate oxide thickness of 500 Å or less. A $P$-base doping concentration to $2.5 \times 10^{17} \text{ cm}^{-3}$ provides a threshold voltage of 4 V in the case of a gate oxide thickness of 500 Å. The $P$-base doping concentration increases to $1.0 \times 10^{18} \text{ cm}^{-3}$ to get the same threshold voltage of 4 V in the case of a gate oxide thickness of 250 Å. These doping levels can be obtained by adjusting the diffusion process used to make the $P$-base and $N^+$ emitter regions as discussed later in the book.

### 3.2 SYMMETRIC IGBT STRUCTURE

The structure for the symmetric blocking, double-diffused, IGBT was shown on the left-hand side of Fig. 2.1. A symmetric blocking, trench-gate, IGBT structure is similar to that shown in Fig. 2.4 without the $N$-buffer layer. The analyses and design procedures described below are applicable to both of these gate structures. The first symmetric blocking IGBT was demonstrated in 1982 [2]. Since the development of IGBT products was mainly focused on motor drive circuits operated from a DC power bus, the symmetric structure lay dormant for nearly 20 years because the asymmetric IGBT structure has much more favorable characteristics for motor drive.
applications. Interest in the symmetric IGBT structure has revived for application in matrix or cyclo-converters [3–6]. The most challenging aspect for development of the symmetric IGBT is a process for edge termination of the reverse blocking junction. This will be discussed in a subsequent chapter on chip design.

### 3.2.1 BLOCKING VOLTAGE

The symmetric IGBT structure can support a high voltage within the $N$-drift region when the collector is biased either positive or negative by the formation of a depletion region across either junction $J_1$ or junction $J_2$. The thickness and doping concentration of the drift region must be optimized to achieve the desired blocking voltage during device structural design. The optimum design depends on the lifetime in the drift region as shown below.

The maximum voltage that the symmetric IGBT structure can support is determined by open-base transistor breakdown [1] because the current generated by leakage and impact ionization is amplified by the gain of the PNP transistor. The open-base transistor breakdown criterion is given by:

$$\alpha_{\text{PNP}} = (\gamma \cdot \alpha_T)_{\text{PNP}} M = 1$$  \hspace{1cm} (3.3)

where $\gamma$ is the injection efficiency of the PN junction ($J_1$ or $J_2$), $\alpha_T$ is the base transport factor, and $M$ is the multiplication factor. The magnitude of $\alpha_T$ and $M$ is a strong function of the collector bias voltage.

The base transport factor ($\alpha_T$) can be computed using:

$$\alpha_T = \frac{1}{\cosh(l/L_p)}$$  \hspace{1cm} (3.4)

where the width ($l$) of the undepleted portion of the $N$-drift region is given by:

$$l = W_N - \sqrt{\frac{2\varepsilon_S V_C}{qN_D}}.$$  \hspace{1cm} (3.5)

In this equation, $\varepsilon_S$ is the dielectric constant of the semiconductor, $V_C$ is the applied bias to the collector electrode, $q$ is the electron charge, and $L_p$ is the diffusion length for holes in the $N$-drift region. The width of the undepleted portion of the $N$-drift region decreases when the collector bias is increased resulting in an increase in the base transport factor.

The multiplication factor can be determined using:

$$M = \left(\frac{1}{1 - (V_C/BV_{PP})^n}\right)^n$$  \hspace{1cm} (3.6)

where $BV_{PP}$ is the avalanche breakdown voltage of the PN junction. A value of $n = 6$ should be used for the case of an $n$-channel IGBT structure. The multiplication factor increases with increasing collector voltage.
An example of the design procedure for optimization of the drift region doping concentration and width for the symmetric blocking IGBT structure with a blocking capability of 3000 V is shown in Fig. 3.3. A low-level lifetime of 10 μs was used in the N-drift region during this analysis. In this figure, the blocking voltage capability has been computed for a given drift region doping concentration (e.g., $2.0 \times 10^{13}$ cm$^{-3}$) for various drift region thickness values. It can be seen that the blocking voltage increases with increasing drift region thickness. The procedure is then repeated for other drift region concentrations. A breakdown voltage of 3300 V, indicated by the dashed line in the figure, provides a 10% margin during device design. It can be observed that many combinations of the drift region doping concentration and width can be used to obtain this blocking voltage capability.

The width of the drift region then increases to 510 μm for a doping concentration of $3.5 \times 10^{13}$ cm$^{-3}$. It can be concluded that a minimum thickness for the N-drift region can be achieved by optimization of the doping concentration. A smaller drift region thickness favors smaller on-state voltage drop and reduced switching losses due to smaller stored charge.

For any desired blocking voltage capability for the symmetric IGBT structure, there is an optimum drift region doping concentration with a corresponding minimum drift region width. These values depend upon the low-level lifetime in the drift region. For the case of device with blocking voltage capability of 3000 V, the drift...
The on-state voltage drop for the IGBT is lower than that for power MOSFETs with the same voltage rating due to the high-level injection of free carriers into the drift region. The voltage drop contributed by the drift region becomes dominant in devices with fast turn-off characteristics. The free carrier distribution in the drift region of the IGBT is an important factor in determining its on-state characteristics.

A schematic illustration of the free carrier distribution in the IGBT structure in the on-state is shown in Fig. 3.5 at two locations in the basic cell cross-section. The carrier distribution on the left-hand side pertains to the location of the deep $P^+$ region in the cell. The carrier distribution on the right-hand side pertains to the location of the gate electrode in the cell. It can be observed that the carrier concentration...
$p_0$ at the collector junction $J_1$ and through most of the drift region is the same for both cases. However, the free carrier concentration is reduced to zero at junction $J_2$ because it is reverse biased during the on-state mode of operation of the IGBT while it becomes enhanced near the gate electrode due to the formation of an accumulation layer produced by the positive gate bias. Since the reduced conductivity modulation of the drift region near the emitter side increases the voltage drop in this portion, it is prudent to utilize the carrier distribution on the left-hand side during on-state analysis to provide a more conservative value for the on-state voltage drop for the IGBT structure.

One-dimensional analysis of the free carrier distribution profile under the deep $P^+$ region is obtained by solving the continuity equation for minority carriers under steady-state high-level injection conditions [1]:

$$\frac{d^2p}{dy^2} - \frac{p}{L_a^2} = 0$$  \hspace{1cm} (3.7)

where $L_a$ is the ambipolar diffusion length in the $N$-base region given by:

$$L_a = \sqrt{D_{a^*}HL}$$  \hspace{1cm} (3.8)

The boundary conditions are

$$p(0) = p_0$$  \hspace{1cm} (3.9)

due to the injection of holes from the $P^+$ collector/$N$-base junction ($J_1$), and

$$p(W_N) = 0$$  \hspace{1cm} (3.10)
due to the reverse biased deep $P^+/N$-base junction ($J_2$). Using these boundary conditions yields:

$$p(y) = p_0 \frac{\sinh[(W_N - y)/L_a]}{\sinh(W_N/L_a)}$$  \hspace{1cm} (3.11)

The hole concentration ($p_0$) at the $P^+$ collector/N-base junction ($J_1$) can be related to collector current ($J_C$) by using [1]:

$$p_0 = \frac{J_C L_a}{2qD_p} \left( \frac{\mu_p}{\mu_n} \right) \tanh(W_N/L_a) \left[ \left( \frac{\mu_n}{\mu_p} \right) \gamma_{E,ON} - (1 + \gamma_{E,ON}) \right]$$  \hspace{1cm} (3.12)

with the injection efficiency at junction $J_1$ in the on-state given by:

$$\gamma_{E,ON} = \frac{J_p}{J_C} = 1 - \frac{J_n}{J_C}$$ \hspace{1cm} (3.13)

where $J_p$ and $J_n$ are the hole and electron current densities at junction $J_1$, and $J_C$ is the total collector current density. The electron current density at junction $J_1$ can be determined using:

$$J_n = \frac{qD_n E \mu_p^2}{L_n E N_{AE}}$$ \hspace{1cm} (3.14)

Combining these equations yields a quadratic solution for the hole concentration ($p_0$) at the $P^+$ collector/N-base junction:

$$a p_0^2 + b p_0 + c = 0$$ \hspace{1cm} (3.15)

where

$$a = \frac{qD_n E}{L_n E N_{AE} J_C} \left( 1 + \frac{\mu_n}{\mu_p} \right)$$ \hspace{1cm} (3.16)

$$b = \frac{2qD_p}{L_a J_C \tanh(W_N/L_a)} \left( \frac{\mu_n}{\mu_p} \right)$$ \hspace{1cm} (3.17)

$$c = -\left( \frac{\mu_n}{\mu_p} \right)$$ \hspace{1cm} (3.18)

The hole concentration ($p_0$) at the $P^+$ collector/N-base junction can be computed using:

$$p_0 = \frac{-b}{2a} \left[ 1 - \sqrt{1 - \left( \frac{4ac}{b^2} \right)} \right]$$ \hspace{1cm} (3.19)
The injected hole concentration for this structure is shown in Fig. 3.6 for the case of four values of the high-level lifetime ($\tau_{HL}$). The doping concentration and thickness for the drift region for the device were chosen to be $2.5 \times 10^{13}$ cm$^{-3}$ and 450 $\mu$m. A doping concentration of $1 \times 10^{19}$ cm$^{-3}$ was used for the $P^+$ collector region with an electron diffusion length of 0.5 $\mu$m inside this region. The highest injected hole concentration (indicated by $p_0$ in the figure) occurs at the $P^+$/N-base junction ($J_1$) with a value of over $10^{17}$ cm$^{-3}$ which is well above the doping concentration of the drift region. The hole concentration reduces to zero at the deep $P^+$/N-base junction ($J_2$) at $y = 450$ $\mu$m. The injected hole concentration becomes smaller throughout the drift region when the lifetime is reduced. This implies a larger voltage drop across the drift region which will also result in a larger on-state voltage drop.

The on-state voltage drop for the IGBT structure can be obtained from the injected carrier distribution shown above after accounting for the voltage drop across the PN junction $J_1$ and the MOSFET region. These voltage drops can be expressed as:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET}$$  \hspace{1cm} (3.20)

where $V_{P+N}$ is the voltage drop across the $P^+$ collector/N-base junction ($J_1$), $V_{NB}$ is the voltage drop across the $N$-base region after accounting for conductivity modulation due to high-level injection conditions, and $V_{MOSFET}$ is the voltage drop across the MOSFET portion.

**FIGURE 3.6**

Distribution of injected holes within the 3000-V symmetric IGBT structure.
The voltage drop across the $P^+$ collector/\(N\)-base junction (\(J_1\)) is given by [1]:

\[
V_{P^+N} = \frac{kT}{q} \ln \left( \frac{p_0N_D}{n_i^2} \right) \tag{3.21}
\]

where the \(n_i\) is the intrinsic carrier concentration. The voltage drop across the \(N\)-base region (\(V_{NB}\)) is obtained by integration of the electric field within the \(N\)-base region. The voltage drop in the drift region is the sum of two terms, \(V_{NB1}\) and \(V_{NB2}\) [1]:

\[
V_{NB1} = \frac{2L_aJ_C \sinh(W_N/L_a)}{q\rho_0(\mu_n + \mu_p)} \left\{ \tanh^{-1} \left[ e^{-(W_{on}/L_a)} \right] - \tanh^{-1} \left[ e^{-(W_n/L_a)} \right] \right\} \tag{3.22}
\]

and

\[
V_{NB2} = \frac{kT}{q} \left( \frac{\mu_n - \mu_p}{\mu_n + \mu_p} \right) \ln \left[ \frac{\tan(W_{ON}/L_a)\cosh(W_{ON}/L_a)}{\tan(W_{N}/L_a)\cosh(W_{N}/L_a)} \right] \tag{3.23}
\]

where \(W_{ON}\) is the depletion width across the reverse biased deep $P^+/N$-base junction (\(J_2\)) in the on-state. The voltage drop across the MOSFET portion consists of contributions from the JFET region, the accumulation layer and the channel. In high voltage IGBT structures, the doping concentration of the JFET region is increased to reduce its contribution to the on-state voltage drop. The JFET region can be assumed to have an effective (uniform) doping concentration of \(5 \times 10^{15}\) cm\(^{-3}\) based upon a Gaussian doping profile with a surface concentration of \(1 \times 10^{16}\) cm\(^{-3}\). The resistivity ($\rho_{JFET}$) for the JFET region is typically 1.25 \(\Omega\)-cm.

Based upon the analysis for the power MOSFET structure [1]:

\[
V_{JFET} = J_C \rho_{JFET}(x_{JP} + W_0)W_{CELL} \tag{3.24}
\]

\[
V_{ACC} = J_C K_A(W_G - 2x_{JP})W_{CELL} \tag{3.25}
\]

\[
V_{CH} = J_C L_{CH} W_{CELL} \tag{3.26}
\]

where \(x_{JP}\) is the junction depth of the \(P\)-base region, \(W_0\) is the depletion width in the JFET region, \(W_G\) is the gate width, \(W_{CELL}\) is the width of the IGBT cell structure, \(K_A\) is the accumulation layer coefficient (typical value 0.6), \(\mu_{nA}\) is the mobility for electrons in the accumulation layer, \(C_{OX}\) is the gate oxide specific capacitance, \(V_G\) is the gate bias voltage, \(V_{TH}\) is the threshold voltage, and \(\mu_{ni}\) is the mobility for electrons in the channel.

The on-state voltage drop obtained by using the above equations is shown in Fig. 3.7 for the case of the 3000-V symmetric IGBT structure. The device has the same parameters for the structure that were used to generate Fig. 3.6 for the injected free carrier concentration. The cell pitch ($W_{CELL}$) of the IGBT structure was 30 \(\mu\)m.
with a gate electrode width \((W_G)\) of 16 \(\mu\)m. The gate bias and threshold voltages used were 15 and 5 V, respectively. The on-state voltage drop is observed to increase rapidly when the high-level lifetime is reduced below 5 \(\mu\)s. This limits the maximum switching speed for the 3000-V symmetric IGBT structure. The figure also provides all the components contributing to the on-state voltage drop. The voltage drop across the \(P^+\) collector/\(N\)-base junction and the MOSFET portion are dominant when the high-level lifetime is large \((>20 \mu\)s\). When the high-level lifetime is reduced, the voltage drop across the \(N\)-base region increases and becomes dominant for lifetime value below 10 \(\mu\)s.

### 3.2.3 STORED CHARGE

The presence of a high concentration of injected carriers within the drift region of the symmetric IGBT structure is regarded as stored charge produced by the on-state current flow. The stored charge must be removed during the turn-off transient to switch the IGBT from the on-state to the forward blocking mode. The stored charge in the drift region can be expected to become smaller when the lifetime is reduced because the hole concentration decreases as shown in Fig. 3.6.

The stored charge in the drift region can be computed by integration of the free carrier distribution given by Eqn (3.11) [1]:

\[
Q_S = \frac{qp_0L_a}{\tanh(W_N/L_a)}
\]  
(3.27)
When the lifetime is reduced in the drift region of the symmetric IGBT structure, the stored charge decreases due to a smaller value for the hole concentration $p_0$ at junction $J_1$ and due to the smaller ambipolar diffusion length.

The stored charge obtained by using the above equation is shown in Fig. 3.8 for the case of the 3000-V symmetric IGBT structure when the high-level lifetime is varied. A rapid growth in the stored charge for lifetime values above 10 $\mu$s is beneficial for reducing the on-state voltage drop but is problematic from the switching loss standpoint as shown below.

### 3.2.4 TURN-OFF SWITCHING WAVEFORMS

IGBTs are commonly used to control inductive loads such as the winding of motors used in a wide variety of consumer and industrial applications. The power circuit consists of the IGBT and the inductive load connected in series with the DC power source, with a free-wheeling or fly-back diode across the load to transfer the current when the IGBT is turned-off. During the turn-off transient, the voltage across the IGBT structure first increases to the collector bias supply voltage before the collector current transfers to the diode.

The collector current initially remains at the on-state value due to the inductive load when the gate voltage is reduced to zero to begin the turn-off transient. The collector current is sustained during this time by the bipolar current in the PNP transistor because the channel current is cut off. During the first phase of the turn-off
process, the collector voltage increases until it reaches the collector supply voltage. The voltage is supported within the IGBT structure by the formation of a space-charge region at the $P$-base/$N$-base junction ($J_2$) with a large concentration of holes in the space-charge layer.

Analysis of the turn-off waveforms for the symmetric IGBT structure can be performed under the assumption that recombination in the $N$-base region can be neglected [1]. In the absence of recombination in the drift region, the free carrier (hole) distribution within the lightly doped portion of the $N$-base region during on-state operation becomes linear as shown at the bottom of Fig. 3.9:

$$p(y) = p_0 \left( 1 - \frac{y}{W_N} \right)$$  \hspace{1cm} (3.28)

The hole profile does not change during the first phase of the turn-off process. Consequently, the concentration of holes at the edge of the space-charge region ($p_e$) increases during the turn-off process because the space-charge width increases:

$$p_e(t) = p_0 \left[ \frac{W_{SC}(t)}{W_N} \right]$$  \hspace{1cm} (3.29)

![FIGURE 3.9](image)

**FIGURE 3.9**

Stored charge and electric field distributions for inductive-load turn-off conditions in a symmetric IGBT structure.
The charge removed by the expansion of the space-charge layer is equal to the charge removed due to collector current flow:

\[ J_{C,ON} = q P_e(t) \frac{dW_{SC}(t)}{dt} = q p_0 \left[ \frac{W_{SC}(t)}{W_N} \right] \frac{dW_{SC}(t)}{dt} \quad (3.30) \]

Integrating this equation with the boundary condition of zero width for the space-charge layer at time zero:

\[ W_{SC}(t) = \sqrt{\frac{2 W_N J_{C,ON} t}{q p_0}} \quad (3.31) \]

The collector voltage supported by the symmetric IGBT structure can be derived from the space-charge layer width:

\[ V_C(t) = \frac{q (N_D + p_{SC}) W_{SC}^2(t)}{2 \varepsilon_S} \quad (3.32) \]

where the hole concentration in the space-charge layer \( p_{SC} \) is given by

\[ p_{SC} = \frac{J_{C,ON}}{q v_{sat,p}} \quad (3.33) \]

under the assumption that the carriers are moving at the saturated drift velocity \( (v_{sat,p}) \) in the space-charge layer. Using Eqn (3.31):

\[ V_C(t) = \frac{W_N (N_D + p_{SC}) J_{C,ON} t}{\varepsilon_S p_0} \quad (3.34) \]

This equation predicts a linear increase in the collector voltage with time during the first phase of the turn-off process for the symmetrical IGBT structure.

The collector voltage reaches the collector supply voltage \( (V_{CS}) \) at the end of the first phase of the turn-off process. The time \( (t_{V,OFF}) \) for the duration of the first phase is:

\[ t_{V,OFF} = \frac{\varepsilon_S p_0 V_{CS}}{W_N (N_D + p_{SC}) J_{C,ON}} \quad (3.35) \]

The width of the space-charge layer at the end of the first phase is:

\[ W_{SC}(t_{V,OFF}) = \sqrt{\frac{2 \varepsilon_S V_{CS}}{q (N_D + p_{SC})}} \quad (3.36) \]

This width is less than the width \( (W_N) \) of the \( N \)-base region because the collector supply voltage is less than the blocking voltage and because the width is reduced by the presence of holes in the space-charge region. Consequently, a large concentration of holes remains in the conductivity-modulated portion of the \( N \)-base region at the end of the first phase.

The decay of the collector current after the voltage rise-time is determined by the recombination of the excess holes and electrons that are trapped within the \( N \)-base
region in the vicinity of the $P^+$ collector/N-base junction [1]. The continuity equation for holes in the N-base region in the absence of diffusion is given by:

$$\frac{d\delta p_N}{dt} = -\frac{\delta p_N}{\tau_{HL}}$$

(3.37)

where $\delta p_N$ is the excess hole concentration in the N-base region. The solution for this equation is:

$$\delta p_N(t) \approx p_N(t) = p_0 e^{-t/\tau_{HL}}.$$  

(3.38)

The collector current flow that supports the recombination of carriers within the stored charge region can be analyzed by examination of the carrier distribution on both sides of the $P^+$ collector/N-base junction ($J_1$). The high concentration of electrons in the N-base region produces the injection of electrons into the $P^+$ collector region. These injected electrons diffuse away from the junction producing an exponential decay in concentration [1].

The collector current produced by the diffusion of the injected electrons in the $P^+$ collector side of the junction is given by:

$$J_C(t) = \frac{qD_nE_0^2}{L_mEN_AE} e^{-2t/\tau_{HL}} = J_{C,ON} e^{-2t/\tau_{HL}}.$$  

(3.39)

It can be concluded that the collector current decreases exponentially with time with a time constant of one-half of the high-level lifetime in the drift region. The collector current turn-off time ($t_{I,OFF}$), defined as the time taken for the current to decay to one-tenth of the on-state value, is given by:

$$t_{I,OFF} = \frac{\tau_{HL}}{2} \ln(10) = 1.15\tau_{HL}$$  

(3.40)

The turn-off waveforms for the case of the 3000-V symmetric IGBT structure with N-base region with a width of 450 μm and a doping concentration of $2.5 \times 10^{13}$ cm$^{-3}$ can be obtained by using the above analytical model. The hole concentration in the space-charge layer is $6.25 \times 10^{13}$ cm$^{-3}$ for on-state collector current density of 100 A/cm$^2$. Three cases of the high-level lifetime are considered here. The hole concentrations ($p_0$) at the $P^+$ collector/N-base junction in the on-state are $1.26 \times 10^{17}$ cm$^{-3}$, $1.67 \times 10^{17}$ cm$^{-3}$, and $1.95 \times 10^{17}$ cm$^{-3}$ for high-level lifetime values of 2, 5 and 10 μs, respectively. The collector voltage and current transients obtained by using these values are shown in Fig. 3.10. The collector voltage increases linearly with time with a collector voltage rise-time ($t_{V,OFF}$) of 0.66, 0.88, and 1.03 μs for high-level lifetime values of 2, 5 and 10 μs, respectively. The collector current then decays exponentially with a collector current turn-off time ($t_{I,OFF}$) of 2.30, 5.75, and 11.5 μs for high-level lifetime values of 2, 5 and 10 μs, respectively. The turn-off switching waveforms and power losses can be controlled by altering the lifetime in the drift region. This is usually accomplished by using high energy (3 MeV) electron irradiation.
3.2.5 TURN-OFF POWER LOSS

From the switching waveforms shown in Fig. 3.10 for the symmetric IGBT structure, it can be concluded that the transients occur with large values for the collector voltage and current. This produces significant instantaneous power loss. From the device design standpoint, it is useful to compute the energy loss occurring during each turn-off transient. The power loss incurred in the IGBT structure in any application can then be computed by multiplying the energy loss per switching cycle with the operating frequency.

The energy loss per cycle can be derived by integration of the power loss during the voltage and current transients. The collector voltage increases linearly with time during the first phase of the turn-off process while the collector current density remains constant for an inductive load. The energy loss per cycle during the first phase of the turn-off process for the symmetric IGBT structure can be calculated using [1]:

\[ E_{V,\text{OFF}} = \frac{1}{2} J_{C,\text{ON}} V_{CSTM,\text{OFF}} \]  

\[ (3.41) \]

The collector current decreases exponentially with time while the collector voltage remains at the collector supply voltage during the second phase of the turn-off process. The energy loss during the current transient can be calculated by using [1]:

\[ E_{I,\text{OFF}} = J_{C,\text{ON}} V_{CS} \left( \frac{\tau_{HL,N-\text{Base}}}{2} \right) \]  

\[ (3.42) \]
The total energy loss per cycle \( E_{OFF} \) is obtained by the addition of these two terms, \( E_{V,OFF} \) and \( E_{I,OFF} \).

The energy loss per cycle for the case of the 3000-V symmetric IGBT structure with \( N \)-base region with a width of 450 \( \mu \)m and a doping concentration of \( 2.5 \times 10^{13} \) \( \text{cm}^{-3} \) can be obtained by using the above analytical model for the case of an on-state collector current density of 100 \( \text{A/cm}^2 \) and collector supply voltage of 2000 \( \text{V} \). The results calculated for high-level lifetime values ranging from one to 100 \( \mu \)s are provided in Fig. 3.11. For the lowest value of the high-level lifetime of 2 \( \mu \)s, the energy loss during the voltage transient is 66 \( \text{mJ/cm}^2 \) while the energy loss during the current transient is 200 \( \text{mJ/cm}^2 \). The energy loss during the voltage transient increases gradually to 131 \( \text{mJ/cm}^2 \) when the high-level lifetime is increased to 100 \( \mu \)s. In contrast, the energy loss during the current transient increases dramatically to 10,000 \( \text{mJ/cm}^2 \) when the high-level lifetime is increased to 100 \( \mu \)s. The total energy loss for the turn-off transient is dominated by the energy loss during the current transient. The high-level lifetime must be kept below 10 \( \mu \)s to limit the total energy loss to below 1 \( \text{J/cm}^2 \).

### 3.2.6 POWER LOSS TRADE-OFF CURVE

The optimization of the design of an IGBT requires trading off the on-state power loss with the turn-off switching power loss. For devices designed for working in circuits operating at lower frequencies, it is appropriate to minimize the on-state voltage drop by using a large lifetime in the drift region. In contrast, for devices...
designed for operating in high frequency circuits, it is appropriate to minimize the turn-off switching energy per cycle. This trade-off is usually performed by making a trade-off curve between on-state voltage drop and energy loss per cycle.

The trade-off curve for the 3000-V symmetric blocking IGBT structure with 450 μm wide N-base region determined by using the equations provided in the previous sections is shown in Fig. 3.12. For the case of an on-state current density of 100 A/cm$^2$, the energy loss per cycle is found to be quite large—in the range of 1 J/cm$^2$. If the switching power loss is limited to 100 W/cm$^2$ by the packaging technology, this would limit the operating frequency of the device to below 100 Hz. The 3000-V symmetric blocking IGBT structure can be operated at a higher frequency if the on-state current density is reduced. This is demonstrated in Fig. 3.12 with trade-off curves for on-state current densities of 25, 50, and 100 A/cm$^2$. A reduction in the on-state current density reduces not only the on-state voltage drop but also the energy loss per cycle because of a reduction of the injected free carrier concentration. The maximum operating frequency can be increased approximately proportional to the reduction in the on-state current density. This will of course require larger chip active area for a given current rating for the device.

3.3 ASYMMETRIC IGBT STRUCTURE

The structure for the asymmetric, double-diffused, IGBT was shown on the left-hand side of Fig. 2.3 and an asymmetric, trench-gate, IGBT structure was shown in Fig. 2.4. The discussion in this section is applicable for both types of gate structures.
The asymmetric IGBT structure was developed soon after the symmetric device structure [7]. The asymmetric structure has much superior trade-off curve between on-state voltage drop and switching loss when compared with the symmetric IGBT structure. Consequently, most of the worldwide effort in the 1980s and 1990s was focused on development of the asymmetric device structure [8–11]. The asymmetric IGBT structure has seen widespread applications in motor drives for air conditioning and refrigeration, in lighting, and in transportation. The voltage ratings of silicon devices have been scaled up rapidly from the initial 600-V capability reported in 1982 to 6500-V capability as shown in Fig. 1.5.

3.3.1 BLOCKING VOLTAGE

The asymmetric IGBT structure can support a high voltage within the $N$-drift region for positive collector voltages. As in the case of the symmetric blocking IGBT structure, the maximum voltage that the asymmetric IGBT structure can support is determined by open-base transistor breakdown using the criterion given by Eqn (3.3). However, the presence of the buffer layer requires alterations of the equations used to determine the thickness of the drift region. In the asymmetric IGBT structure, the injection efficiency of the $P^+$ collector/$N$-buffer junction ($J_1$) is given by [1]:

$$\gamma_E = \frac{D_{pNB}L_{nE}N_{AE}}{D_{pNB}L_{nE}N_{AE} + D_{nE}W_{NB}N_{DNB}}$$  \hspace{1cm} (3.43)

where $D_{pNB}$ and $D_{nE}$ are the diffusion coefficients for minority carriers in the $N$-buffer and $P^+$ collector regions; $N_{AE}$ and $L_{nE}$ are the doping concentration and diffusion length for minority carriers in the $P^+$ collector region; $N_{DNB}$ and $W_{NB}$ are the doping concentration and width of the $N$-buffer layer.

In the asymmetric IGBT structure, the depletion layer extends through the lightly doped drift region at a relatively low collector voltage well below the breakdown voltage of the structure. Consequently, the minority carriers need to diffuse through only the $N$-buffer layer. The base transport factor is therefore given by:

$$\alpha_T = \frac{1}{\cosh\left(W_{NB}/L_{p,NB}\right)}$$  \hspace{1cm} (3.44)

where $L_{p,NB}$ is the diffusion length for holes in the $N$-buffer layer and $W_{NB}$ is the width of the buffer layer. The diffusion length for holes ($L_{p,NB}$) in the $N$-buffer layer depends upon the diffusion coefficient and the minority carrier lifetime in the $N$-buffer layer which are both dependent upon the doping concentration in the $N$-buffer layer [1].

The multiplication factor for the asymmetric IGBT structure is determined by the collector bias relative to the avalanche breakdown voltage of the deep $P^+$ region/$N$-base junction ($BV_{PP}$) without the punch-through phenomenon. The multiplication coefficient can be computed by using [1]:

$$M = \frac{1}{1 - \left(V_{NPT}/BV_{PP}\right)^{\eta}}$$  \hspace{1cm} (3.45)
where \( n = 6 \) for the case of a \( P^+/N \) diode. In this expression, the nonpunch-through voltage \( (V_{NPT}) \) can be computed from the applied collector bias by using [1]:

\[
V_{NPT} = \frac{\varepsilon_S}{2qN_D} \left( \frac{V_C}{W_N} + \frac{qN_D W_N}{2\varepsilon_S} \right)^2
\]  

(3.46)

The forward blocking capability of the asymmetric IGBT structure is determined by the collector voltage at which the multiplication factor becomes equal to the reciprocal of the product of the base transport factor and the emitter injection efficiency.

Any desired forward blocking capability can be achieved in the asymmetric IGBT structure by appropriate combination of the drift region doping, drift region thickness, buffer layer doping, and buffer layer thickness. During the optimization of the design, it is preferable to achieve the smallest thickness for the drift region in order to reduce the on-state voltage drop and the stored charge. The change in the thickness of the drift region with drift region doping concentration to achieve a forward blocking voltage of 3300 V is shown in Fig. 3.13 for the case of a buffer layer thickness of 10 \( \mu \)m. Here, the buffer layer doping was used as a parametric variable. It can be observed that for each buffer layer doping concentration the drift region thickness has a minimum value. In all three cases, the minimum drift region thickness occurs at the same optimum drift region doping concentration of \( 1 \times 10^{13} \) cm\(^{-3} \). The optimum drift region thickness is 279, 258, and 246 \( \mu \)m for the buffer layer doping concentrations of \( 0.5 \times 10^{17} \), \( 1.0 \times 10^{17} \) cm\(^{-3} \), and

---

**FIGURE 3.13**

Optimizing drift region thickness for the asymmetric IGBT structure: \( N \)-buffer doping as parametric variable.
The smallest drift region thickness is achieved for the highest buffer layer doping concentration because this produces the smallest injection efficiency and base transport factor.

The change in the thickness of the drift region with drift region doping concentration to achieve a forward blocking voltage of 3300-V is shown in Fig. 3.14 for the case of a buffer layer doping concentration of \(1.0 \times 10^{17} \text{ cm}^{-3}\). Here, the buffer layer thickness was used as a parametric variable. It can be observed that for each buffer layer thickness the drift region thickness has a minimum value. In all three cases, the minimum drift region thickness occurs at the same optimum drift region doping concentration of \(1 \times 10^{13} \text{ cm}^{-3}\). The optimum drift region thickness is 287, 258, and 234 \(\mu\text{m}\) for the buffer layer thicknesses of 5, 10, and 20 \(\mu\text{m}\), respectively. The smallest drift region thickness is achieved for the largest buffer layer thickness because this produces the smallest injection efficiency and base transport factor.

### 3.3.2 ON-STATE CHARACTERISTICS

The free carrier distribution in the asymmetric IGBT structure determines its on-state voltage drop. As in the case of the symmetric IGBT structure, the free carrier distribution in the \(N\)-drift region can be altered by changing the lifetime. However, in the case of the asymmetric IGBT structure, the free carrier distribution can also be changed by altering the doping concentration and thickness of the \(N\)-buffer layer. This provides more latitude for optimization of the structure during its design for
a particular application. In general, the optimization requires finding the free carrier distribution that provides the combination of on-state voltage drop and turn-off time that produces the lowest power loss in the intended circuit application.

One-dimensional analysis of the free carrier distribution profile under the deep $P^+$ region for this structure can be obtained by solving the continuity equation (see Eqn (3.7)) for minority carriers under steady-state high-level injection conditions [1]. The boundary condition on the emitter side is the same as that for the symmetric structure (see Eqn (3.10)). However, the boundary condition on the collector side is different for the asymmetric IGBT structure due to the presence of the buffer layer.

An analytical model has been developed for the asymmetric IGBT structure which is valid for any injection level in the buffer layer [12]. In this model, the hole and electron concentrations in the $N$-base region are assumed to be equal due to charge neutrality and the low doping concentration required for the drift region. The on-state carrier distribution profile for the asymmetric IGBT structure is shown in Fig. 3.15 indicating an abrupt change in the hole concentration at the boundary between the $N$-drift region and the $N$-buffer layer. In the $N$-buffer layer, the hole concentration is comparable to the doping concentration ($N_{DB}$).

The hole concentration ($p_{NB}(0)$) in the buffer layer at junction ($J_1$) can be obtained by solution of the following quadratic equation [12]:

$$p_{NB}^2(0) + \left( \frac{D_{pNB}N_{AP+} + D_{nP+}N_{DB}L_{pNB}}{D_{nP+}L_{pNB}} \right) p_{NB}(0) - \frac{N_{AP+}L_{nP+}J_C}{qD_{nP+}} = 0 \quad (3.47)$$

The solution of this equation is:

$$p_{NB}(0) = \frac{1}{2} \left( \sqrt{b^2 - 4c} - b \right) \quad (3.48)$$
where

\[
b = \frac{D_{pNB} N_{AP^+} L_{nP^+} + D_{nP^+} N_{DBL} L_{pNB}}{D_{nP^+} L_{pNB}} \quad (3.49)
\]

and

\[
c = \frac{N_{AP^+} L_{nP^+} J_C}{q D_{nP^+}} \quad (3.50)
\]

Here, \(D_{pNB}\) is the diffusion coefficient for holes in the buffer layer, \(N_{AP^+}\) is the acceptor doping concentration of the \(P^+\) collector region, \(L_{nP^+}\) is the diffusion length for electrons in the collector region, \(D_{nP^+}\) is the diffusion coefficient for electrons in the collector region, \(N_{DB}\) is the donor doping concentration in the buffer layer, and \(L_{pNB}\) is the diffusion length for holes in the buffer layer.

The hole concentration \(p(W_{NB^-})\) inside the buffer layer at the boundary between the \(N\)-buffer layer and the \(N\)-base region is given by [12]:

\[
p(W_{NB^-}) = p_{NB}(0) e^{-\left(\frac{W_{NB}}{L_{pNB}}\right)} \quad (3.51)
\]

where \(W_{NB}\) is the thickness of the buffer layer. The hole concentration \(p(W_{NB^+})\) in the \(N\)-base region at the boundary between the \(N\)-buffer layer and the \(N\)-base region can be obtained by using [2]:

\[
p(W_{NB^+}) = \frac{L_a \tanh[(W_N + W_{NB})/L_a]}{2qD_p} J_p(W_{NB^-}) \quad (3.52)
\]

with the current density

\[
J_p(W_{NB^-}) = J_p(0) e^{-\left(\frac{W_{NB}}{L_{pNB}}\right)} \quad (3.53)
\]

The hole concentration profile in the \(N\)-drift region can be computed using [2]:

\[
p(y) = p(W_{NB^+}) \frac{\sinh[(W_N + W_{NB} - y)/L_a]}{\sinh[(W_N + W_{NB})/L_a]} \quad (3.54)
\]

The hole carrier distribution obtained by using the above equations is shown in Fig. 3.16 for the case of the 3000-V asymmetric IGBT structure when the lifetime in the drift region is altered. Based upon the breakdown voltage analysis, an \(N\)-base region thickness of 280 \(\mu\)m was chosen, with a buffer layer doping concentration of \(1.0 \times 10^{17}\) cm\(^{-3}\) and buffer layer thickness of 10 \(\mu\)m. The injected hole concentration remains well above the doping concentration of \(1 \times 10^{13}\) cm\(^{-3}\) for the \(N\)-drift region when the high-level lifetime is above 2 \(\mu\)s. At high-level lifetime value of 2 \(\mu\)s and below, the hole concentration in the drift region on the emitter side becomes much lower than at the collector side. This produces an increase in the on-state voltage drop.

The on-state voltage drop for the asymmetric IGBT structure can be obtained by using [12]:

\[
V_{ON} = V_{P+NBL} + V_B + V_{MOSFET} \quad (3.55)
\]
where $V_{P+NBL}$ is the voltage drop across the $P^+$ collector/$N$-buffer layer junction ($J_1$), $V_B$ is the voltage drop across the $N$-base region after accounting for conductivity modulation due to high-level injection conditions, and $V_{MOSFET}$ is the voltage drop across the MOSFET portion. Since the junction ($J_1$) between the $P^+$ collector region and the $N$-buffer layer operates at neither high-level nor low-level injection conditions, the voltage drop across the junction ($J_1$) must be obtained using:

$$V_{P+NB} = \frac{kT}{q} \ln \left( \frac{p_{NB}(0)N_{BL}}{n_i^2} \right)$$ \hspace{1cm} (3.56)

The voltage drop across the $N$-base region is given by the sum of two terms, $V_{B1}$ and $V_{B2}$ [12]:

$$V_{B1} = \frac{2 L_a J_C \sinh(W_N/L_a)}{q p(W_{NB+}) \left( \mu_n + \mu_p \right)} \left\{ \tanh^{-1} \left[ e^{-(W_{ON}/L_a)} \right] - \tanh^{-1} \left[ e^{-(W_N/L_a)} \right] \right\}$$ \hspace{1cm} (3.57)

and

$$V_{B2} = \frac{kT}{q} \left( \frac{\mu_n - \mu_p}{\mu_n + \mu_p} \right) \ln \left[ \frac{\tanh(W_{ON}/L_a) \cosh(W_{ON}/L_a)}{\tanh(W_N/L_a) \cosh(W_N/L_a)} \right]$$ \hspace{1cm} (3.58)
where $W_{OV}$ is the depletion width across the $P$-base/$N$-base junction ($J_2$) in the on-state. The voltage drop across the MOSFET portion is given by the same equations previously provided for the asymmetric blocking IGBT structure.

The on-state voltage drop obtained by using the above equations is shown in Fig. 3.17 for the case of the 3000-V asymmetric IGBT structure when the high-level lifetime is varied from 1 to 100 $\mu$s in the $N$-drift region. The device has the same parameters for the structure that were used to generate Fig. 3.16 for the injected free carrier concentration. The cell pitch ($W_{CELL}$) of the IGBT structure was 30 $\mu$m with a gate electrode width ($W_G$) of 16 $\mu$m. The gate bias and threshold voltages used were 15 and 5 V, respectively. The on-state voltage drop is observed to increase rapidly when the high-level lifetime is reduced below 2 $\mu$s. This lifetime is three times smaller than that for the 3000-V symmetric IGBT structure because the drift region width is much larger for the symmetric IGBT structure. The figure also provides all the components contributing to the on-state voltage drop. The voltage drop across the $P^+$ collector/$N$-base junction and the MOSFET portion are dominant when the high-level lifetime is large (>5 $\mu$s). When the high-level lifetime is reduced, the voltage drop across the $N$-base region increases and becomes dominant for lifetime value below 3 $\mu$s.

As mentioned earlier, the asymmetric IGBT structure can be optimized by varying the doping concentration in the $N$-buffer layer. This is illustrated in Fig. 3.18 for the case of the 3000-V asymmetric IGBT structure with a high-level lifetime of 5 $\mu$s.

**FIGURE 3.17**

Components of the on-state voltage drop for the 3000-V asymmetric IGBT.
The buffer layer thickness was kept fixed at 10 μm. It can be observed that the hole concentration \( [p_{NB}(0)] \) decreases from \( 9.7 \times 10^{16} \) to \( 4.7 \times 10^{16} \) cm\(^{-3}\) when the buffer layer doping is increased from \( 5 \times 10^{17} \) to \( 5 \times 10^{16} \) cm\(^{-3}\). This produces a reduced injected hole concentration throughout the drift region as well. A smaller hole concentration in the drift region in the on-state will increase the on-state voltage drop and reduce the turn-off time.

The on-state voltage drop (at an on-state current density of 100 A/cm\(^2\)) computed for the 3000-V asymmetric silicon IGBT structure by using the above equations is provided in Fig. 3.19 as a function of the doping concentration of the buffer layer. This structure had the same parameters for the drift region as used for the carrier distribution in Fig. 3.18. A high-level lifetime of 5 μs was used for the graph. It can be observed that the on-state voltage drop increases rapidly when the \( N \)-buffer layer doping is increased beyond \( 5 \times 10^{17} \) cm\(^{-3}\) due to a rapid increase in the voltage drop across the \( N \)-drift region.

The on-state voltage drop computed for the 3000-V asymmetric silicon IGBT structure at an on-state current density of 100 A/cm\(^2\) is provided in Fig. 3.20 as a function of the doping concentration of the buffer layer for various values of the high-level lifetime in the \( N \)-drift region. This structure had a buffer layer thickness of 10 μm. It can be observed that the on-state voltage drop increases rapidly when the \( N \)-buffer layer doping is increased beyond a certain level for each of the values
FIGURE 3.19
On-state voltage drop components for the 3000-V asymmetric IGBT structure: $N$-buffer layer doping dependence.

FIGURE 3.20
On-state voltage drop for the 3000-V asymmetric IGBT structure: $N$-buffer layer doping dependence.
for the high-level lifetime in the N-buffer layer. This level of the N-buffer layer doping concentration becomes smaller when the high-level lifetime is reduced.

The asymmetric IGBT structure can also be optimized by varying the thickness of the N-buffer layer. This is illustrated in Fig. 3.21 for the case of the 3000-V asymmetric IGBT structure with a high-level lifetime of 5 μs. The buffer layer doping concentration was kept fixed at $1 \times 10^{17}$ cm$^{-3}$ in this example. It can be observed that the hole concentration [$p_{NB}(0)$] is independent of the buffer layer thickness. However, the hole concentration in the drift region decreases when the buffer layer thickness is increased because of the longer path for the diffusion of holes from junction $J_1$ to the interface between the buffer layer and the drift region. A smaller hole concentration in the drift region in the on-state will increase the on-state voltage drop and reduce the turn-off time.

The on-state voltage drop (at an on-state current density of 100 A/cm$^2$) computed for the 3000-V asymmetric silicon IGBT structure by using the above equations is provided in Fig. 3.22 as a function of the thickness of the buffer layer. This structure had the same parameters for the drift region as used for the carrier distribution in Fig. 3.21. A high-level lifetime of 5 μs was used for the graph. It can be observed that the on-state voltage drop increases gradually when the N-buffer layer thickness is increased from 5 to 50 μm.

The on-state voltage drop computed for the 3000-V asymmetric silicon IGBT structure at an on-state current density of 100 A/cm$^2$ is provided in Fig. 3.23 as a

![Figure 3.21](image-url)

**FIGURE 3.21**
Hole carrier distribution in the 3000-V asymmetric IGBT structure: buffer layer thickness dependence.
Figure 3.22
On-state voltage drop components for the 3000-V asymmetric IGBT structure: N-buffer layer thickness dependence.

Figure 3.23
On-state voltage drop for the 3000-V asymmetric IGBT structure: N-buffer layer thickness dependence.
function of the thickness of the buffer layer for various values of the high-level lifetime in the $N$-drift region. This structure had a buffer layer doping concentration of $1 \times 10^{17}$ cm$^{-3}$. It can be observed that the on-state voltage drop is weakly dependent on the buffer layer thickness when the high-level lifetime in the drift region is large (10 $\mu$s in this example). However, the on-state voltage drop increases rapidly when the $N$-buffer layer thickness is increased when the high-level lifetime in the drift region is reduced to 2 $\mu$s. These graphs indicate that all the parameters for the asymmetric IGBT must be adjusted to obtain an optimized structure.

### 3.3.3 STORED CHARGE

As in the case of the symmetric IGBT structure, the stored charge in the drift region must be removed during the turn-off transient to switch the asymmetric IGBT from the on-state to the forward blocking mode. The free carrier distribution in the drift region of the asymmetric IGBT was discussed in the previous section and shown to be dependent on the lifetime in the drift region and the buffer layer doping and thickness. The stored charge in the drift region can be computed by integration of the free carrier distribution given by Eqn (3.54) [1]:

$$Q_S = \frac{q p (W_{NB+} + L_a) \tanh(W_N/L_a)}{\tanh(W_N/L_a)}$$  \hspace{1cm} (3.59)

The stored charge obtained by using the above equation is shown in Fig. 3.24 for the case of the 3000-V asymmetric IGBT structure when the high-level lifetime in

![FIGURE 3.24](image)

Stored charge in the 3000-V asymmetric IGBT structure: drift region lifetime dependence.
the drift region is varied. The parameters used for this device structure are the same as those used to generate the on-state voltage drop in Fig. 3.17. A rapid growth in the stored charge for lifetime values above 10 μs is beneficial for reducing the on-state voltage drop but is problematic from the switching loss standpoint as shown below.

The stored charge obtained for the case of the 3000-V asymmetric IGBT structure is provided in Fig. 3.25 when the N-buffer layer doping concentration is varied. The parameters used for this device structure are the same as those used to generate the on-state voltage drop in Fig. 3.19 with a high-level lifetime of 5 μs in the drift region. It can be observed that the stored charge is a weak function of the buffer layer doping concentration until it exceeds $1 \times 10^{17}$ cm$^{-3}$. A rapid reduction in the stored charge occurs when the buffer layer doping concentration exceeds $1 \times 10^{17}$ cm$^{-3}$ but this accompanied by a rapid increase in the on-state voltage drop as observed in Fig. 3.19.

The stored charge for the case of the 3000-V asymmetric IGBT structure is shown in Fig. 3.26 when the N-buffer layer thickness is varied. The parameters used for this device structure are the same as those used to generate the on-state voltage drop in Fig. 3.22 with a high-level lifetime of 5 μs in the drift region. It can be observed that the stored charge can be monotonically reduced by increasing the buffer layer thickness. A gradual change occurs in both the stored charge and on-state voltage drop when the buffer layer thickness is altered indicating that it is a good design parameter for optimization of asymmetrical IGBT structures.

![Graph showing stored charge vs N-buffer layer doping concentration](image)
3.3.4 TURN-OFF SWITCHING WAVEFORMS

The analysis of the turn-off waveforms for the asymmetric IGBT structure can be performed using the same approach as used for the symmetric IGBT structure in Section 3.2.4 [1,12]. For the asymmetric IGBT structure, the hole concentration in the drift region can be approximated by:

\[ p(y) = p_{WN}^+ \left( 1 - \frac{y}{W_N} \right) \]  \hfill (3.60)

It will be assumed that the above hole distribution does not change during the first phase when the collector voltage increases during the turn-off process. Consequently, the concentration of holes at the edge of the space-charge region \( p_e \) increases with time as the space-charge width increases:

\[ p_e(t) = p_{WN}^+ \left[ \frac{W_{SC}(t)}{W_N} \right] \]  \hfill (3.61)

The expansion of the space-charge layer with time, as indicated by the horizontal time arrow in Fig. 3.27, is then obtained using the same approach as for the symmetric structure:

\[ W_{SC}(t) = \sqrt{\frac{2 W_N J_{C,ON} t}{qp_{WN}^+}} \]  \hfill (3.62)
The collector voltage supported by the asymmetric IGBT structure can be calculated from the space-charge layer width:

$$V_C(t) = \frac{q(N_D + p_{SC})W_{SC}^2(t)}{2\varepsilon_S}$$  \hspace{1cm} (3.63)$$

where the hole concentration in the space-charge layer is related to the collector current density:

$$p_{SC} = \frac{J_{C,ON}}{qv_{sat,p}}$$  \hspace{1cm} (3.64)$$

Using Eqn (3.62) in Eqn (3.63):

$$V_C(t) = \frac{W_N(N_D + p_{SC})J_{C,ON}}{\varepsilon_S p_{WNB}^+ t}$$  \hspace{1cm} (3.65)$$

which indicates a linear increase in the collector voltage with time. The first phase is completed when the collector voltages reach the collector supply voltage (V_{CS}). This
time interval \( t_{V,OFF} \) can be obtained by making the collector voltage equal to the collector supply voltage in Eqn (3.65):

\[
t_{V,OFF} = \frac{\varepsilon_{SPWB} + V_{CS}}{W_N(N_D + p_{SC})J_{C,ON}}
\] (3.66)

The width of the space-charge layer at the end of the first phase depends upon the collector supply voltage. In most asymmetric IGBT designs, the width of the space-charge layer is slightly less than the width of the drift region for typical collector supply voltage values for which the IGBT has been designed.

The collector current decays during the second phase of the turn-off process. The rate of change of the collector current is governed by recombination of the stored charge remaining after the collector voltage transient. There is only stored charge in the buffer layer during the current decay because the stored charge in the drift region has been removed during the voltage rise-time. The stored charge in the buffer layer decays by recombination as indicated by the vertical time arrow in Fig. 3.27:

\[
\delta p_{NB}(t) \approx p_{0}e^{-t/\tau_{p0,NB}}
\] (3.67)

because low-level injection conditions prevail in the N-buffer layer during most of the decay. Based upon this, the collector current density is given by [1]:

\[
J_{C}(t) = J_{C,ON}e^{-t/\tau_{p0,NB}}
\] (3.68)

The collector current turn-off time \( t_{I,OFF} \) is defined as the time taken for the current to decay to one-tenth of the on-state value. It can be computed using:

\[
t_{I,OFF} = \tau_{p0,NB} \ln(10) = 2.3\tau_{p0,NB}
\] (3.69)

The turn-off waveforms for the 3000-V asymmetric IGBT structure with N-base region with a lightly doped portion with a width of 280 \( \mu \)m and a doping concentration of \( 1 \times 10^{13} \) \( \text{cm}^{-3} \), a buffer layer width of 10 \( \mu \)m, and a doping concentration of \( 1 \times 10^{17} \) \( \text{cm}^{-3} \) are shown in Fig. 3.28 for the case of three high-level lifetime values in the drift region. The collector voltage increases linearly with time with a collector voltage rise-time \( t_{V,OFF} \) of 0.615, 1.06, and 1.40 \( \mu \)s for high-level lifetime values of 2, 5, and 10 \( \mu \)s, respectively. The collector current then decays exponentially with a collector current turn-off time \( t_{I,OFF} \) of 0.77, 1.92, and 3.83 \( \mu \)s for high-level drift-region lifetime values of 2, 5, and 10 \( \mu \)s, respectively. This demonstrates that the turn-off switching waveforms and power losses can be controlled by altering the lifetime in the drift region. This is usually accomplished by using high energy (3 MeV) electron irradiation.

The switching loss during turn-off for the asymmetric IGBT can also be controlled by varying the doping concentration in the buffer layer. This is demonstrated for the case of the 3000-V asymmetric IGBT structure with N-base region with a lightly doped portion with a width of 280 \( \mu \)m and a doping concentration of \( 1 \times 10^{13} \) \( \text{cm}^{-3} \), a buffer layer width of 10 \( \mu \)m, and high-level lifetime of 5 \( \mu \)s in the drift region. It can be observed in Fig. 3.29 that the collector voltage
FIGURE 3.28
Collector current and voltage transients during turn-off for the asymmetric IGBT structure with an inductive load: lifetime dependence.

FIGURE 3.29
Collector current and voltage transients during turn-off for the asymmetric IGBT structure with an inductive load: buffer doping dependence.
rise-time \((t_{V,OFF})\) can be reduced from 1.06 to 0.648 to 0.424 \(\mu s\) when the buffer layer doping concentration is increased from 1.0 to 3.0 to \(5.0 \times 10^{17} \text{ cm}^{-3}\), respectively. The collector current decays exponentially with a collector current turn-off time \((t_{I,OFF})\) of 1.92, 0.821, and 0.523 \(\mu s\) for these values of the buffer layer doping, respectively. This demonstrates that the buffer layer doping concentration can be utilized as a sensitive design parameter for optimization of the turn-off switching waveforms and power losses for the asymmetric IGBT. This is usually accomplished by controlling the doping during epitaxial growth for lower blocking voltage devices or by the addition of a diffused \(n\)-type layer from the collector side of the wafer.

The turn-off transients for the asymmetric IGBT can also be altered by varying the thickness of the buffer layer. This is demonstrated for the case of the 3000-V asymmetric IGBT structure with \(N\)-base region with a lightly doped portion with a width of 280 \(\mu m\) and a doping concentration of \(1 \times 10^{13} \text{ cm}^{-3}\), a buffer layer doping concentration of \(1 \times 10^{17} \text{ cm}^{-3}\), and high-level lifetime of 5 \(\mu s\) in the drift region. It can be observed in Fig. 3.30 that the collector voltage rise-time \((t_{V,OFF})\) can be reduced from 1.06 to 0.679 to 0.434 \(\mu s\) when the buffer layer doping thickness is increased from 10 to 20 to 30 \(\mu m\), respectively. In all of these cases, the collector current decays exponentially with a collector current turn-off time \((t_{I,OFF})\) of 1.92 \(\mu s\) because the lifetime in the buffer layer has the same value. This example demonstrates that the buffer layer thickness can be utilized as another design parameter for optimization of the turn-off switching waveforms and power losses for the asymmetric IGBT. The thickness of the buffer layer can be easily controlled during

![FIGURE 3.30](image)

Collector current and voltage transients during turn-off for the asymmetric IGBT structure with an inductive load: buffer thickness dependence.
epitaxial growth for lower blocking voltage devices or by adjusting the diffusion time for an $n$-type layer from the collector side of the wafer.

### 3.3.5 TURN-OFF POWER LOSS

The energy loss per cycle during the first phase of the turn-off process ($E_{V,OFF}$) for the asymmetric IGBT structure can be calculated using Eqn (3.41) because the voltage waveform during turn-off for the asymmetric IGBT is similar to that for the symmetric IGBT structure. The energy loss during the current transient for the asymmetric IGBT can be calculated by using [12]:

\[
E_{I,OFF} = J_{C,ON} V C S \tau_{\text{p0},N-Buffer} \quad (3.70)
\]

The total energy loss per cycle ($E_{OFF}$) is obtained by the addition of these two terms ($E_{V,OFF}$ and $E_{I,OFF}$).

The energy loss per cycle for the case of the 3000-V asymmetric IGBT structure with $N$-base region with a width of 280 $\mu$m and a doping concentration of $1.0 \times 10^{13}$ cm$^{-3}$, buffer layer thickness of 10 $\mu$m, and a doping concentration of $1.0 \times 10^{17}$ cm$^{-3}$ can be obtained by using the above analytical model for the case of an on-state collector current density of 100 A/cm$^2$ and collector supply voltage of 2000-V. The results calculated for high-level lifetime values ranging from 1 to 100 $\mu$s are provided in Fig. 3.31. For the lowest value of the high-level lifetime of 2 $\mu$s, the energy loss during the voltage transient is 62 mJ/cm$^2$ while the energy

![Asymmetric IGBT Structure](image)

**FIGURE 3.31**

Energy loss during the turn-off transient for the asymmetric 3000-V IGBT structure: lifetime dependence.
loss during the current transient is 67 mJ/cm². The energy loss during the voltage transient increases gradually to 141 mJ/cm² when the high-level lifetime is increased to 100 μs. In contrast, the energy loss during the current transient increases dramatically to 3480 mJ/cm² when the high-level lifetime is increased to 100 μs. The total energy loss for the turn-off transient is dominated by the energy loss during the current transient. The high-level lifetime must be kept below 10 μs to limit the total energy loss to below 0.5 J/cm². The energy loss per cycle for the asymmetric IGBT structure is much less than that for the symmetric IGBT structure (see Fig. 3.11).

The energy loss per cycle for the 3000-V asymmetric IGBT structure can be controlled by changing the buffer layer doping concentration. The energy loss obtained by using the above analytical model for the case of an on-state collector current density of 100 A/cm² and collector supply voltage of 2000-V is shown in Fig. 3.32 for the case of a high-level lifetime of 5 μs in the drift region and buffer layer thickness of 10 μm. At buffer layer doping levels below $1 \times 10^{17}$ cm⁻³, the energy loss during the current transient is found to be dominant. At buffer layer doping levels above $1 \times 10^{17}$ cm⁻³, the energy loss during the voltage and current transients are found to be equal. The energy loss monotonically reduces with increasing buffer layer doping concentration providing a good design variable when optimizing the asymmetric IGBT structure.

The energy loss per cycle for the above 3000-V asymmetric IGBT structure is shown in Fig. 3.33 as a function of the buffer layer doping concentration for various
values for the high-level lifetime in the drift region. The energy loss was calculated using the above analytical model for the case of an on-state collector current density of 100 A/cm² and collector supply voltage of 2000-V. In all cases, the energy loss decreases monotonically with increasing buffer layer doping concentration. From these plots, it can be observed that the design of the asymmetric IGBT can be optimized by using an optimum combination of high-level lifetime in the drift region and the buffer layer doping concentration.

The energy loss per cycle for the 3000-V asymmetric IGBT structure can also be controlled by changing the buffer layer thickness. The energy loss obtained by using the above analytical model for the case of an on-state collector current density of 100 A/cm² and collector supply voltage of 2000-V is shown in Fig. 3.34 for the case of various high-level lifetime values in the drift region while using a buffer layer doping concentration of $1 \times 10^{17}$ cm⁻³. The energy loss decreases with increasing buffer layer thickness for each value for the high-level lifetime. The gradual monotonic reduction in energy loss with increasing buffer layer thickness allows control of the energy loss using buffer layer thickness as a design parameter.

### 3.3.6 POWER LOSS TRADE-OFF CURVE

As mentioned before, the trade-off curve between on-state voltage drop and turn-off energy per cycle allows optimization of the IGBT structure for any particular application. The trade-off curve obtained by varying the high-level lifetime in the drift region...
region for the 3000-V asymmetric blocking IGBT structure is shown in Fig. 3.35 for the case of an on-state current density of 100 A/cm² and collector supply voltage of 2000-V during switching. This device structure has a drift region width of 280 μm and a doping concentration of $1 \times 10^{13}$ cm⁻³, a buffer layer width of 10 μm, and a doping concentration of $1 \times 10^{17}$ cm⁻³. If the switching power loss is limited to 100 W/cm² by the packaging technology, the asymmetric IGBT would be limited to an operating frequency below 500 Hz based upon an energy loss per cycle of 0.2 J/cm². The operating frequency for the 3000-V asymmetric IGBT is found to be five times larger than that for the 3000-V symmetric IGBT structure for an on-state current density of 100 A/cm². This is the reason asymmetric IGBT structures are preferred for typical motor drive applications.

A trade-off curve between on-state voltage drop and turn-off energy per cycle can be developed for the asymmetric IGBT structure by varying the doping concentration of the buffer layer. The trade-off curve obtained using this approach for the 3000-V asymmetric blocking IGBT structure is shown in Fig. 3.36 for the case of various high-level lifetime values in the drift region. An on-state current density of 100 A/cm² and collector supply voltage of 2000-V during switching was used for generating these trade-off curves. This device structure has a drift region width of 280 μm and a doping concentration of $1 \times 10^{13}$ cm⁻³ and a buffer layer width of 10 μm. It can be observed that the trade-off curve shifts toward the left-hand side when the lifetime in the drift region is increased producing a superior trade-off curve. If the switching power loss is limited to 100 W/cm² by the packaging technology, the operating frequency for the asymmetric IGBT would be limited to 500 Hz based upon an energy loss per cycle of 0.2 J/cm². The operating frequency for the 3000-V asymmetric IGBT is found to be five times larger than that for the 3000-V symmetric IGBT structure for an on-state current density of 100 A/cm². This is the reason asymmetric IGBT structures are preferred for typical motor drive applications.

![Energy loss during the turn-off transient for the asymmetric 3000-V IGBT structure: buffer layer thickness dependence.](image-url)
FIGURE 3.35
Trade-off curves for the asymmetric 3000-V IGBT structure: drift lifetime variation.

FIGURE 3.36
Trade-off curves for the asymmetric 3000-V IGBT structure: buffer doping variation.
technology, the asymmetric IGBT would be limited to an operating frequency below 1000 Hz based upon an energy loss per cycle of 0.1 J/cm². This demonstrates the ability to improve the performance of the asymmetric IGBT structure by the optimum combination of the drift region lifetime and the buffer layer doping concentration. It is worth pointing out that the best combination of on-state voltage drop and energy loss per cycle occurs for a high-level lifetime of 10 μs in the drift region with a relatively high buffer layer doping concentration of $5 \times 10^{17}$ cm⁻³.

The asymmetric IGBT structure can also be optimized by variation of the thickness of the buffer layer. This is demonstrated in Fig. 3.37 for the case of the 3000-V asymmetric IGBT structure a drift region width of 280 μm, a doping concentration of $1 \times 10^{13}$ cm⁻³, and a buffer layer doping concentration of $1 \times 10^{17}$ cm⁻³. Various values for the drift region high-level lifetime were used during this optimization. In this case, a composite trade-off curve can be created as shown in Fig. 3.37 by the dashed line representing the best trade-off curve obtainable with this approach.

As in the case of the symmetric blocking structure, the asymmetric IGBT structure can operate at a higher frequency if the on-state current density is decreased because both the on-state voltage drop and energy loss per cycle are reduced. This is demonstrated in Fig. 3.38 with trade-off curves achieved by varying the buffer layer doping concentration for on-state current densities of 100, 50 and 25 A/cm². In all cases a high-level lifetime of 10 μs was used for the drift region because this produces the best trade-off curve as previously shown with the aid of
The maximum operating frequency can be increased approximately proportional to the reduction in the on-state current density. This will of course require larger chip active area for a given current rating for the device.

The maximum operating frequency for the IGBT is limited by the power dissipation which produces a rise in temperature within the chip. For reliable operation, it is typical to limit the total power dissipation density to 200 W/cm² in order to maintain a junction temperature of 125 °C. The total power dissipated by the IGBT is given by the sum of the on-state and switching power loss:

\[ P_L = 0.5J_{C,ON}V_{ON} + E_{OFF}f \]  

for the case of a 50% duty cycle if the turn-on power loss is neglected. The maximum operating frequency is the given by:

\[ f_{Max} = \left( \frac{P_{L,Max} - 0.5J_{C,ON}V_{ON}}{E_{OFF}} \right) \]  

where \( P_{L,Max} \) is the maximum power dissipation and \( V_{ON} \) is the on-state voltage drop. The maximum operating frequency for the 3000-V asymmetric IGBT structure whose trade-off curves were shown in Fig. 3.38 are provided in Fig. 3.39. For the case of an on-state current density of 100 A/cm², a peak of 900 Hz is observed for the maximum operating frequency when the buffer layer doping concentration is increased to \( 1 \times 10^{18} \) cm⁻³. This peak moves to a value of 4000 Hz at a buffer layer doping concentration is increased to \( 2 \times 10^{18} \) cm⁻³ when the on-state current...
density is reduced to 50 A/cm². For an on-state current density of 25 A/cm², a maximum operating frequency beyond 10-kHz can be achieved for this 3000-V asymmetric IGBT structure. The desired increase in operating frequency is achieved at the expense of a larger chip size for the intended application.

3.4 TRANSPARENT EMITTER IGBT STRUCTURE

The structure for the transparent emitter IGBT was shown on the left-hand side of Fig. 2.5 together with the doping profile on the right-hand side. The DMOS-gate structure for the device is similar to the previous structures and can be replaced by the trench-gate structure as well. The unique aspect of the transparent emitter IGBT structure is its very thin and more lightly doped collector region. The term “transparent” refers to the ability of electrons injected into the collector region to diffuse to the collector contact due to its small thickness. The term “emitter” is used because the collector region of the IGBT actually serves as the emitter of the internal PNP transistor. The smaller dopant charge in the collector region reduces the injection efficiency at junction $J_1$ allowing a reduction of the stored charge in the drift region.

The transparent emitter concept was first applied to the IGBT structure in the 1990s when the effort was directed toward very high (4.5-kV) blocking voltage
structures for traction applications [13—17]. When the capability to handle thinner wafers during device processing became possible, the idea was extended to lower blocking voltages as well, including devices with 600-V forward blocking capability fabricated from 60-μm thick silicon wafers.

### 3.4.1 Blocking Voltage

It is typical to include a buffer layer in the transparent emitter IGBT structure and to use a high lifetime within the drift region. The buffer layer has also been referred to as a “field-stop” layer because the electric field punches-through the drift region until its spread is stopped by the higher doping level of the buffer layer. With the inclusion of a buffer layer, the analysis of the blocking voltage for the transparent emitter IGBT becomes similar to that for the asymmetric IGBT structure as described in detail in Section 3.3.1. The drift region can be optimized using an appropriate combination of the drift region doping concentration and thickness. In the case of a 3000-V IGBT structure, a drift region doping concentration of $1 \times 10^{13}$ cm$^{-3}$, and thickness of 280 μm are suitable with a typical buffer layer thickness of 10 μm.

### 3.4.2 On-State Characteristics

A generally applicable analytical model for the asymmetric IGBT structure which is valid for any injection level in the buffer layer was previously proposed [12]. This analytical model is extended to the transparent emitter IGBT structure with a buffer layer here.

A schematic illustration of the carrier profile in the on-state for the transparent emitter IGBT structure is shown in Fig. 3.40. The thickness of the $P$-collector region ($W_{P+}$) is small when compared with the previous structures. Consequently, the

![FIGURE 3.40](image)

On-state carrier distribution in the transparent emitter IGBT structure.
diffusion length for the electrons injected into the collector region is much greater than its thickness. The electron profile in the collector region then becomes linear from an injected concentration of $n_C(0)$ at the junction to zero at the metal contact. The hole and electron concentrations in the $N$-base region are equal due to charge neutrality. The hole concentration in the $N$-buffer layer is comparable to the doping concentration ($N_{DB}$) in the buffer layer. Consequently, the electron concentration in the buffer becomes larger than the doping concentration to preserve charge neutrality. The electron concentration ($n_{NB}(0)$) in the buffer layer at the junction ($J_1$) is given by:

$$n_{NB}(0) = N_{DB} + p_{NB}(0)$$

Using the Boltzmann quasi-equilibrium boundary condition for the carrier densities on both sides of the junction ($J_1$) together with Eqn (3.73):

$$\frac{p_C}{p_{NB}(0)} = \frac{n_{NB}}{n_C(0)} = \frac{N_{DB} + p_{NB}}{n_C(0)}$$

For a uniformly doped collector region, the hole concentration ($p_C$) is equal to the doping concentration ($N_{AP+}$) because it is operating under low-level injection conditions. In the case of a diffused collector region, an effective doping concentration is given by:

$$N_{AEP+} = 20\sqrt{N_{AES}N_D}$$

should be used where $N_{AES}$ is the surface concentration of the collector diffusion [1].

From Eqn (3.74):

$$n_C(0) = \frac{N_{DB}p_{NB}(0) + p_{NB}^2(0)}{N_{AEP+}}$$

For the transparent emitter structure, the linear electron carrier profile results in the electron current density at junction ($J_1$) given by:

$$J_n(0) = \frac{qD_{nP+}}{W_{P+}} n_C(0)$$

where $D_{nP+}$ is the diffusion coefficient for electrons in the $P^+$ collector region, and $W_{P+}$ is its thickness. The hole current density at junction ($J_1$) is given by:

$$J_p(0) = \frac{qD_{pNB}}{L_{pNB}} p_{NB}(0)$$

where $D_{pP+}$ and $L_{pP+}$ are the diffusion coefficient and diffusion length for holes in the buffer layer, respectively. All the parameters in these equations must be calculated after taking into account the reduction of the mobility and lifetime in the highly doped buffer layer and collector. The total collector current density is the sum of these components:

$$J_C = J_n(0) + J_p(0) = \frac{qD_{nP+}}{W_{P+}} n_C(0) + \frac{qD_{pNB}}{L_{pNB}} p_{NB}(0)$$
Using Eqn (3.76), an expression for the hole concentration in the buffer layer at junction ($J_1$) can be derived:

$$p_{NB}^2(0) + \left( \frac{D_{pNB}N_{AP}W_{p} + D_{nP}+N_{DB}L_{pNB}}{D_{nP}+L_{pNB}} \right) p_{NB}(0) - \frac{N_{AP}+W_{p}+J_{C}}{qD_{nP}+} = 0 \quad (3.80)$$

The hole concentration in the buffer layer at junction ($J_1$) is the solution of this quadratic equation:

$$p_{NB}(0) = \frac{1}{2} \left( \sqrt{b^2 - 4c} - b \right) \quad (3.81)$$

where

$$b = \frac{D_{pNB}N_{AP}W_{p} + D_{nP}+N_{DB}L_{pNB}}{D_{nP}+L_{pNB}} \quad (3.82)$$

and

$$c = \frac{N_{AP}+W_{p}+J_{C}}{qD_{nP}+} \quad (3.83)$$

The holes concentration ($p(W_{NB-})$) inside the buffer layer at the boundary between the $N$-buffer layer and the $N$-base region is given by:

$$p(W_{NB-}) = p_{NB}(0)e^{-\left(W_{NB}/L_{pNB}\right)} \quad (3.84)$$

where $W_{NB}$ is the thickness of the buffer layer. Due to high-level injection conditions, the hole concentration profile in the $N$-base region is given by [1]:

$$p(y) = p(W_{NB+}) \frac{\sinh\left(\left(W_{N} + W_{NB} - y\right)/L_{a}\right)}{\sinh\left(\left(W_{N} + W_{NB}\right)/L_{a}\right)} \quad (3.85)$$

for $y > W_{NB}$. In this expression, the hole concentration ($p(W_{NB+})$) in the $N$-base region at the boundary between the $N$-buffer layer and the $N$-base region can be obtained by equating the hole current density on the two sides of this boundary [1]:

$$p(W_{NB+}) = \frac{L_{a} \tanh\left(\left(W_{N} + W_{NB}\right)/L_{a}\right)}{2qD_{p}} J_{p}(W_{NB-}) \quad (3.86)$$

with

$$J_{p}(W_{NB-}) = J_{p}(0)e^{-\left(W_{NB}/L_{pNB}\right)} \quad (3.87)$$

The on-state carrier distribution obtained by using the above equations is provided in Fig. 3.41 for the case of the 3000-V transparent emitter IGBT structure with a collector region thickness of 1 μm and a doping concentration of $1 \times 10^{18}$ cm$^{-3}$. A drift region thickness of 280 μm, a buffer layer thickness of 10 μm, and high-level lifetime ($\tau_{HL}$) in the drift region of 20 μs were used in this example. It can be observed that the hole concentrations $p_{NB}(0)$ and $p_{WNB+}$ decrease with increasing buffer layer doping. In comparison with the asymmetric IGBT
structure, the hole concentration in the drift region for the transparent emitter structure is reduced for all cases by about a factor of three times on the collector side of the drift region in spite of the two times larger lifetime in the drift region. This is due to the reduced injection efficiency of the collector junction created by the transparent emitter. In contrast, the hole concentration in the transparent emitter IGBT structure is about two times larger than for the asymmetric IGBT structure on the emitter side of the drift region due to high value for the lifetime in the drift region.

The on-state carrier distribution can also be adjusted by varying the doping concentration of the collector region in the transparent emitter IGBT structure. This is illustrated in Fig. 3.42 for the case of the 3000-V transparent emitter IGBT structure with a drift region thickness of 280 μm, a buffer layer thickness of 10 μm, a buffer layer doping concentration of $5 \times 10^{16}$ cm$^{-3}$, and high-level lifetime ($\tau_{HL}$) of 20 μs in the drift region. It can be observed that the hole concentrations $p_{NB}(0)$ and $p_{WNB+}$ increase with increasing collector doping concentration due to the enhanced injection efficiency of the collector junction.

As in the case of the previous symmetric and asymmetric IGBT structures, the on-state carrier distribution can be adjusted by varying the lifetime in the drift region of the transparent emitter IGBT structure. This is illustrated in Fig. 3.43 for the case of the 3000-V transparent emitter IGBT structure with a drift region thickness of 280 μm, a buffer layer thickness of 10 μm, a buffer layer doping concentration of $5 \times 10^{16}$ cm$^{-3}$, and a collector doping concentration of $1 \times 10^{18}$ cm$^{-3}$. It can be
FIGURE 3.42
On-state carrier distribution in the 3000-V transparent emitter IGBT structure: collector doping dependence.

FIGURE 3.43
On-state carrier distribution in the 3000-V transparent emitter IGBT structure: drift region lifetime dependence.
observed that the hole concentrations $p_{NB}(0)$ and $p_{WNB+}$ decrease when the lifetime in the drift region is reduced.

The on-state voltage drop for the transparent emitter IGBT structure can be obtained by using the equations provided in Section 3.2.2 for the asymmetric IGBT structure. The influence of changing the buffer layer doping concentration, the collector doping concentration, and the lifetime in the drift region is discussed here for the case of the 3000-V structure.

The components of the on-state voltage drop for the 3000-V transparent emitter IGBT structure at an on-state current density of 100 A/cm² are shown in Fig. 3.44 as a function of the buffer layer doping concentration. This structure has a collector region thickness of 1 µm and a doping concentration of $1 \times 10^{18}$ cm⁻³, a drift region thickness of 280 µm, buffer layer thickness of 10 µm, and high-level lifetime ($\tau_{HL}$) in the drift region of 20 µs. The on-state voltage drop increases rapidly for this structure when the buffer layer doping concentration exceeds $1 \times 10^{17}$ cm⁻³ because of the rapid increase in the voltage drop ($V_{NB}$) across the drift region.

For the case of a high-level lifetime of 20 µs in the drift region, the on-state voltage drop increases relatively slowly with increasing buffer layer doping concentration as shown in Fig. 3.44. This does not hold true when the lifetime in the drift region is reduced as shown in Fig. 3.45. It can be observed that the on-state voltage drop becomes too large at high buffer layer doping concentration when the high-level lifetime is reduced to 5 µs. This is the reason for using relatively high lifetime
values for the drift region in the transparent emitter IGBT structure and utilizing the collector doping concentration to optimize the injected hole concentration in the drift region.

The impact of varying the collector doping concentration in the transparent emitter IGBT structure is illustrated for the case of the 3000-V structure in Fig. 3.46. This structure has a collector region thickness of 1 μm, a drift region thickness of 280 μm, a buffer layer thickness of 10 μm, and high-level lifetime ($\tau_{HL}$) in the drift region of 20 μs. It can be observed that the on-state voltage drop becomes too large at high buffer layer doping concentrations when the collector doping level is reduced below $1 \times 10^{18}$ cm$^{-3}$.

3.4.3 STORED CHARGE

The free carrier distribution in the drift region of the transparent emitter IGBT structure was discussed in the previous section and shown to be dependent on the collector doping concentration, the lifetime in the drift region, and the buffer layer doping concentration. The stored charge in the drift region can be computed by using Eqn (3.59).

The stored charge computed for the case of the 3000-V transparent emitter IGBT structure is provided in Fig. 3.47 when the buffer layer doping concentration is varied for various values of the lifetime in the drift region. The parameters used for this
FIGURE 3.46
On-state voltage drop for the 3000-V transparent emitter IGBT structure: collector doping dependence.

FIGURE 3.47
Stored charge in the 3000-V transparent emitter IGBT structure: buffer layer doping dependence with lifetime as parametric variable.
device structure are the same as those used to generate the on-state voltage drop in Fig. 3.45. It can be observed that the stored charge is a weak function of the buffer layer doping concentration until it exceeds $1 \times 10^{17}$ cm$^{-3}$. A rapid reduction in the stored charge occurs when the buffer layer doping concentration exceeds $1 \times 10^{17}$ cm$^{-3}$ but this is accompanied by a rapid increase in the on-state voltage drop as observed in Fig. 3.45. For the same high-level lifetime of 5 $\mu$s in the drift region, the transparent emitter IGBT has three times smaller stored charge at a buffer layer doping concentration of $1 \times 10^{17}$ cm$^{-3}$ than the asymmetrical IGBT structure (see Fig. 3.25).

The stored charge in the transparent emitter IGBT can also be controlled by changing the doping concentration in the collector region. This is demonstrated for the 3000-V structure for the case of a drift region lifetime of 20 $\mu$s in Fig. 3.48. It can be observed that the stored charge increases when the doping concentration of the transparent emitter is increased. This is due to an improvement in the injection efficiency of junction $J_1$.

### 3.4.4 TURN-OFF SWITCHING WAVEFORMS

The analysis of the turn-off waveforms for the transparent emitter IGBT structure can be performed by using the same approach as used for the asymmetric IGBT structure in Section 3.2.4. The voltage transient is given by Eqn (3.65) and the current transient by Eqn (3.68). The turn-off waveforms for the 3000-V transparent
emitter IGBT structure with a $N$-base region width of 280 μm and a doping concentration of $1 \times 10^{13} \text{ cm}^{-3}$, a buffer layer width of 10 μm, and a doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$ are shown in Fig. 3.49 for the case of three collector doping concentrations. A high-level lifetime of 20 μs was used in the drift region in this example. The collector voltage increases linearly with time with a collector voltage rise-time ($t_{V,\text{OFF}}$) that decreases from 0.764 to 0.309 to 0.126 μs when the collector doping concentration is reduced from 5 to 2 to $1 \times 10^{18} \text{ cm}^{-3}$, respectively, because of the reduced injected hole concentration in the drift region. It can be concluded that the collector rise-time can be controlled by altering the doping concentration in the collector region for the transparent emitter IGBT structure. The collector current decays exponentially with a collector current turn-off time ($t_{I,\text{OFF}}$) of 2.09 μs for all three cases because the lifetime in the buffer layer has the same value.

The switching loss during turn-off for the transparent emitter IGBT structure can also be controlled by varying the lifetime in the drift region. This is demonstrated in Fig. 3.50 for the case of the 3000-V structure with $N$-base region width of 280 μm and a doping concentration of $1 \times 10^{13} \text{ cm}^{-3}$, a buffer layer width of 10 μm and doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$, and a collector region width of 1 μm and doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$. It can be observed that the collector voltage rise-time ($t_{V,\text{OFF}}$) can be reduced from 0.126 to 0.105 to 0.074 μs when the drift region high-level lifetime is reduced from 20 to 10 to 5 μs, respectively. The collector current decays exponentially with a collector current turn-off time ($t_{I,\text{OFF}}$) of 2.09,
1.05, and 0.523 μs for these values of the lifetime, respectively. This demonstrates that the drift region lifetime is a sensitive design parameter for optimization of the turn-off switching waveforms and power losses for the transparent emitter IGBT.

The third approach for optimization of the performance of the transparent emitter IGBT is by altering the buffer layer doping concentration. This is demonstrated in Fig. 3.51 for the case of the 3000-V transparent emitter IGBT structure with $N$-base region width of 280 μm and a doping concentration of $1 \times 10^{13}$ cm$^{-3}$, a buffer layer thickness of 10 μm, high-level lifetime of 10 μs in the drift region; and a collector doping concentration of $1 \times 10^{18}$ cm$^{-3}$. It can be observed that the collector voltage rise-time ($t_{V,OFF}$) increases from 0.105 to 0.254 to 0.387 μs when the buffer layer doping concentration is reduced from 5 to 2 to $1 \times 10^{17}$ cm$^{-3}$, respectively, due to an increase in the injected hole concentration in the drift region. The collector current decays exponentially with a collector current turn-off time ($t_{I,OFF}$) that increases from 1.05 to 2.30 to 3.83 μs for these cases because of an increase in the buffer layer lifetime. This example demonstrates that the buffer layer doping concentration can be utilized as another design parameter for optimization of the turn-off switching waveforms and power losses for the transparent emitter IGBT structure. Since the transparent emitter IGBT structure has been employed for very high voltage devices, the buffer layer doping is usually controlled by diffusion of phosphorus from the back-side of the wafer.
3.4.5 TURN-OFF POWER LOSS

The energy loss per cycle for the transparent emitter IGBT structure during the voltage rise-time can be computed using Eqn (3.41) developed for the symmetric structure and during the current fall-time using Eqn (3.70) for the asymmetric IGBT structure. The energy loss per cycle for the case of the 3000-V transparent emitter IGBT structure with \( N \)-base region width of 280 \( \mu \text{m} \) and a doping concentration of \( 1.0 \times 10^{13} \text{ cm}^{-3} \), a buffer layer thickness of 10 \( \mu \text{m} \), and doping concentration of \( 1.0 \times 10^{17} \text{ cm}^{-3} \) obtained by using the above analytical model for the case of an on-state collector current density of 100 A/cm\(^2\) and collector supply voltage of 2000-V is provided in Fig. 3.52. In this plot, three cases of the high-level lifetime in the drift region have been considered. It can be observed that the collector doping concentration can be used as a design variable to determine the energy loss per cycle. The lowest energy loss per cycle occurs for low collector doping concentration because of the reduced injected hole concentration in the drift region. The hole concentration is also reduced when the lifetime is decreased making the energy loss per cycle smaller.

The energy loss per cycle for the transparent emitter IGBT structure can also be controlled by changing the buffer layer doping concentration. The energy loss obtained by using the above analytical model for the case of an on-state collector current density of 100 A/cm\(^2\) and collector supply voltage of 2000-V is shown in Fig. 3.53 for the case of a collector doping concentration of \( 1 \times 10^{18} \text{ cm}^{-3} \). Three

**FIGURE 3.51**
Collector current and voltage transients during turn-off for the transparent emitter IGBT structure with an inductive load: buffer doping dependence.
FIGURE 3.52
Energy loss during the turn-off transient for the transparent emitter 3000-V IGBT structure: collector doping dependence.

FIGURE 3.53
Energy loss during the turn-off transient for the transparent emitter 3000-V IGBT structure: buffer layer doping dependence.
cases of the drift region high-level lifetime are considered in this figure. The energy loss per cycle decreases monotonically with increasing buffer layer doping concentration providing a good design variable when optimizing the transparent emitter IGBT structure. The energy loss per cycle can be greatly reduced by decreasing the lifetime in the drift region.

### 3.4.6 POWER LOSS TRADE-OFF CURVE

The trade-off curve for the 3000-V transparent emitter IGBT structure obtained by varying the collector doping concentration is shown in Fig. 3.54 for the case of an on-state current density of 100 A/cm² and collector supply voltage of 2000 V during switching. This device structure has a drift region width of 280 μm and doping concentration of \(1 \times 10^{13} \text{ cm}^{-3}\), and a buffer layer width of 10 μm and doping concentration of \(1 \times 10^{17} \text{ cm}^{-3}\). Three cases of the high-level lifetime in the drift region are considered in the figure. From the perspective of the trade-off curve, the collector doping is not a good variable because the energy loss per cycle is only weakly dependent on the collector doping concentration as seen in Fig. 3.52. However, it is strongly dependent on the drift region lifetime as seen by the downward shift of the trade-off curve when the lifetime is reduced.

A trade-off curve between on-state voltage drop and turn-off energy per cycle can be developed for the transparent emitter IGBT structure by varying the doping

![Trade-off curves for the transparent emitter 3000-V IGBT structure: collector doping as parametric variable.](image-url)
concentration of the buffer layer. The trade-off curve obtained using this approach for the 3000-V asymmetric blocking IGBT structure is shown in Fig. 3.55 for the case various high-level lifetime values in the drift region. An on-state current density of 100 A/cm$^2$ and collector supply voltage of 2000-V during switching was used for generating these trade-off curves. This device structure has a drift region width of 280 $\mu$m and doping concentration of $1 \times 10^{13}$ cm$^{-3}$, and a buffer layer width of 10 $\mu$m. It can be observed that the trade-off curves for the different lifetime cases overlap. This indicates that the same point on the trade-off curve is produced for multiple combinations of the drift region lifetime and the buffer layer doping concentration.

The maximum operating frequency for the IGBT is limited by the power dissipation which produces a rise in temperature within the chip. The total power dissipation in the IGBT structure is given by Eqn (3.71) for the case of a 50% duty cycle if the turn-on power loss is neglected. Using this equation, the maximum operating frequency is given by Eqn (3.72). For reliable operation, it is typical to limit the total power dissipation density to 200 W/cm$^2$ in order to maintain a junction temperature of 125 $^\circ$C. The maximum operating frequency for the 3000-V transparent emitter IGBT structure, whose trade-off curves were shown in Fig. 3.54, is provided in Fig. 3.56 as a function of the collector doping concentration for three drift region lifetime values. In all three cases, the maximum operating frequency becomes less

![FIGURE 3.55](image-url)

Trade-off curves for the transparent emitter 3000-V IGBT structure: buffer doping as parametric variable.
than zero when the collector doping level becomes too small because the on-state power dissipation exceeds 200 W/cm². It can be concluded that a larger maximum operating frequency can be achieved by reducing the drift region lifetime. There is an optimum collector doping level of about $3 \times 10^{18}$ cm⁻³ at which the maximum operating frequency has its highest value for each lifetime case but this is a broad maxima giving good design and process latitude when making the transparent emitter IGBT structure. It can also be concluded a collector doping concentration of $1 \times 10^{18}$ cm⁻³ is too low because it degrades the maximum operating frequency by half for the case of a high-level lifetime of 5 μs.

The maximum operating frequency for the 3000-V transparent emitter IGBT structure is provided in Fig. 3.57 as a function of the buffer layer doping concentration for three drift region lifetime values. A collector doping concentration of $3 \times 10^{18}$ cm⁻³ was used for these plots because this was found to improve the maximum operating frequency as shown in Fig. 3.56. The maximum operating frequency becomes less than zero when the buffer layer doping level becomes too high because the on-state power dissipation exceeds 200 W/cm². For each lifetime value, there is a well-defined optimum buffer layer doping where the maximum operating frequency has its highest value. It can be concluded that the largest maximum operating frequency can be achieved by using a drift region lifetime of 10 μs and a buffer layer doping concentration of $6 \times 10^{17}$ cm⁻³. This demonstrates the design optimization procedure required to extract the best performance from the transparent emitter IGBT structure.
The maximum operating frequency for the 3000-V transparent emitter IGBT structure can be increased by decreasing the on-state current density because this reduces both the on-state voltage drop and the energy loss per cycle. This requires using a larger chip area to achieve any desired current rating making the cost of the device larger. The maximum operating frequency for the 3000-V transparent emitter IGBT is provided in Fig. 3.58 as a function of the buffer layer doping concentration for three on-state current density values. But a collector doping concentration of $3 \times 10^{18}$ cm$^{-3}$ and drift region high-level lifetime of 10 $\mu$s were used for these plots because this was found to improve the maximum operating frequency as shown in Fig. 3.56. The maximum operating frequency becomes limited to about 1000 Hz for an on-state current density of 100 A/cm$^2$. It can be increased to 3000 and 6500 Hz by reducing the on-state current density to 50 and 25 A/cm$^2$, respectively.

### 3.5 SILICON CARBIDE IGBT STRUCTURES

The development of power devices from silicon carbide (SiC) is motivated by its high breakdown field strength. The specific resistance of the drift region for a vertical power device structure is related to the basic semiconductor properties by [18]:

$$R_{on-specific} = \frac{4BV^2}{\varepsilon_S\mu_pE_C^3}$$  \hspace{1cm} (3.88)
where $BV$ is the breakdown voltage, $\varepsilon_S$ is the dielectric constant, $\mu_n$ is the electron mobility, and $E_C$ is the critical electric field for breakdown. The denominator of this equation is commonly referred to as Baliga’s Figure-of-Merit (BFOM) for semiconductors. Based upon available information about the properties of silicon carbide, a BFOM of about 2000 is predicted for the 4H-SiC polytype [19]. This has motivated the development of SiC unipolar devices, such as Schottky rectifiers [20] (including the JBS structure [21–23]) and power MOSFETs [24–26] in the 1990s. These devices are now commercially available from several companies [27–29].

Excellent SiC unipolar power devices can be created with breakdown voltages up to 5000 V [19]. For applications that requires devices with even larger blocking voltage capability, it is possible to develop IGBTs from silicon carbide. SiC-based IGBTs have the advantages of a much smaller drift region thickness which reduces the on-state voltage drop and the stored charge. The development of $n$-channel SiC IGBTs was hindered by the high resistance of the $P$-type substrates that must serve as the collector region. Consequently, $p$-channel, asymmetric SiC IGBTs were first developed with 99- to 12-kV forward blocking capability using thick $p$-type epitaxial layers grown on highly doped $n$-type substrates [30–32]. A channel mobility of 6.5 $\text{cm}^2/\text{V-s}$ was measured for holes for these devices. Asymmetric $n$-Channel SiC IGBTs were subsequently developed [33] with blocking voltage of 13 kV. A channel mobility of 18 $\text{cm}^2/\text{V-s}$ was measured for electrons for these devices. Analysis of 15 kV symmetric blocking IGBTs has demonstrated [34] that

---

**FIGURE 3.58**

Maximum operating frequency for the transparent emitter 3000-V IGBT structure: on-state current density as parametric variable.
these structures can have competitive performance with asymmetric devices. The blocking voltage capability for p-channel asymmetric 4H-SiC IGBTs has been extended to 15-kV [35]. Comparison between the SiC power MOSFET and the n-channel IGBT for typical motor drive applications [36] suggests that the IGBT structure is superior to the power MOSFET structure when the blocking voltage exceeds 9 kV. This analysis predicts the highest MVA rating for the n-channel SiC IGBT structure at a blocking voltage of 20 kV.

3.5.1 n-CHANNEL ASYMMETRIC SiC IGBT STRUCTURE

The planar, asymmetric, n-channel SiC IGBT structure is shown in Fig. 3.59 together with its doping profile. Unlike the silicon IGBT, the doping concentrations of the various layers are uniform for the SiC devices. Since techniques for controlling the lifetime in the drift region are unavailable, the SiC IGBT structure must be optimized by altering the doping and thickness of the buffer layer [35]. The basic physics of operation for the SiC n-channel asymmetric IGBT structure is identical to that previously discussed for silicon devices in Section 3.2. The equations provided in that section for the blocking voltage design, on-state carrier distribution, on-state voltage drop, and turn-off wave forms can therefore also be applied to the SiC IGBT after taking into account appropriate changes to the basic material properties.

FIGURE 3.59
The SiC n-channel asymmetric IGBT structure with its doping profile.
3.5.2 BLOCKING CHARACTERISTICS

As an example, the design of the 15-kV 4H-SiC n-channel asymmetric IGBT structure is considered in this section. The forward blocking capability of the asymmetric SiC IGBT structure is determined by the open-base transistor breakdown phenomenon. The emitter injection efficiency for the $P^+$ collector/N-buffer junction ($J_1$) can be obtained by using Eqn (3.43). The diffusion coefficients and diffusion length are dependent on the doping concentrations in the $P^+$ collector region and N-buffer layer. Open-base breakdown occurs in the silicon carbide asymmetric IGBT structure when the multiplication coefficient is only slightly above unity. Using the avalanche breakdown criteria when the multiplication coefficient becomes equal to infinity, as assumed in some papers [37], can lead to significant errors during the design of the drift region for the IGBT structure. The minority carrier lifetime has been found to be dependent upon the doping concentration [38] in the case of silicon devices. Although this phenomenon has not been verified for silicon carbide, it is commonly used when performing numerical analysis of SiC devices. The effect can be modeled by using the relationship:

$$\frac{\tau_{LL}}{\tau_{P0}} = \frac{1}{1 + (N_D/N_{REF})}$$  \hspace{1cm} (3.89)

where $N_{REF}$ is a reference doping concentration whose value will be assumed to be $5 \times 10^{16}$ cm$^{-3}$ as done for the silicon devices.

As in the case of silicon devices, the multiplication factor for a $P$-$N$ junction is given by:

$$M = \frac{1}{1 - (V_A/BV_{PP})^n}$$  \hspace{1cm} (3.90)

with a value of $n = 6$ for the case of a $P^+/N$ junction and the avalanche breakdown voltage of the $P$-base/N-base junction ($BV_{PP}$) without the punch-through phenomenon. This breakdown voltage is much larger for SiC devices due to the very high critical electric field for breakdown when compared with silicon. The multiplication coefficient for the asymmetric SiC IGBT structure can be computed by using this nonpunch-through voltage given by Eqn (3.46).

For the 15-kV n-channel asymmetric IGBT structure, the drift region must be designed to achieve a blocking voltage capability of 16.5 kV. In the case of avalanche breakdown, there is a unique value of $6.0 \times 10^{14}$ cm$^{-3}$ for the drift region with a width of 170 μm to obtain this blocking voltage. In the case of the asymmetric SiC IGBT structure, it is advantageous to use a much lower doping concentration for the lightly doped portion of the N-base region in order to reduce its width. The strong conductivity modulation of the N-base region during on-state operation favors a smaller thickness for the N-base region independent of its original doping concentration.

Any desired forward blocking capability can be achieved in the SiC asymmetric IGBT structure by appropriate combination of the drift region doping, drift region...
thickness, buffer layer doping, and buffer layer thickness. During the optimization of the design, it is preferable to achieve the smallest thickness for the drift region in order to reduce the on-state voltage drop and the stored charge. The change in the thickness of the drift region with drift region doping concentration to achieve a forward blocking voltage of 16,500 V is shown in Fig. 3.60 for the case of a buffer layer thickness of 5 μm. Here, the buffer layer doping was used as a parametric variable. A low-level lifetime of 1 μs was assumed in the drift region. It can be observed that for each buffer layer doping concentration the drift region thickness has a minimum value. In all three cases, the minimum drift region thickness occurs at the same optimum drift region doping concentration of $2 \times 10^{14} \text{ cm}^{-3}$. The optimum drift region thickness is 134, 126, and 118 μm for the buffer layer doping concentrations of 1.0, 2.0, and $5.0 \times 10^{17} \text{ cm}^{-3}$, respectively. The smallest drift region thickness is achieved for the highest buffer layer doping concentration because this produces the smallest injection efficiency and base transport factor.

The change in the thickness of the drift region with drift region doping concentration to achieve a forward blocking voltage of 16,500 V is shown in Fig. 3.61 for the case of a buffer layer doping concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$. Here, the buffer layer thickness was used as a parametric variable. A low-level lifetime of 1 μs was assumed in the drift region. It can be observed that for each buffer layer thickness the drift region thickness has a minimum value. The minimum drift region thickness occurs at an optimum drift region doping concentration ranging from 1 to $2 \times 10^{14} \text{ cm}^{-3}$. The optimum drift region thickness is 156, 134, and 122 μm for
the buffer layer thicknesses of 2, 5, and 10 μm, respectively. The smallest drift region thickness is achieved for the largest buffer layer thickness because this produces the smallest injection efficiency and base transport factor.

Based upon the results of the above analysis, it can be concluded that the drift region for a SiC asymmetric IGBT structure should have a doping concentration of $2 \times 10^{14}$ cm$^{-3}$ and thickness of 140 μm to achieve the design target of 16,500-V forward blocking capability. This is the value that has been typically used in making actual SiC asymmetric IGBTs [35].

### 3.5.3 ON-STATE VOLTAGE DROP

The analytical model for the carrier distribution in the drift region and the on-state voltage drop developed for the silicon asymmetric IGBT structure can also be applied to SiC devices. It is of course necessary to apply the appropriate values for the SiC material parameters. One of the major differences between the silicon and SiC structures is that voltage drop across the forward biased $p$-$n$ junction increases from about 0.7 to 3 V. In addition, the lifetime in the drift region of SiC devices has been found to be much lower than in silicon devices but this is compensated by the smaller thickness of the drift region in SiC devices. As a design example, the 15-kV SiC asymmetric IGBT structure will be analyzed here with a drift region having a doping concentration of $2 \times 10^{14}$ cm$^{-3}$ and thickness of 140 μm based upon the analysis described in the previous section.
The carrier distribution in the drift region and buffer layer for the 15-kV asymmetric IGBT structure at an on-state current density of 25 A/cm² is shown in Fig. 3.62 for the case of various high-level lifetime values. A buffer layer with doping concentration of $1 \times 10^{17} \text{cm}^{-3}$ and thickness of 5 μm was assumed here. It can be observed that the carrier concentration falls below the drift region doping level of $2 \times 10^{14} \text{cm}^{-3}$ on the emitter side when the high-level lifetime is reduced below 1 μs. This indicates that an increase in the on-state voltage drop can be expected for this IGBT structure when the high-level lifetime is reduced below 1 μs. The on-state voltage drop for the 15-kV asymmetric IGBT structure obtained by using analytical model is provided in Fig. 6.63 as a function of the high-level lifetime in the drift region. From the various components of the on-state voltage drop in the figure, it is clear that the voltage drop in the drift region increases rapidly once the high-level lifetime is made less than 1 μs.

As in the case of the asymmetric silicon IGBT, the doping concentration of the buffer layer can be used as a design parameter to control its on-state voltage drop. The carrier distribution in the drift region and buffer layer for the 15-kV asymmetric IGBT structure at an on-state current density of 25 A/cm² is shown in Fig. 3.64 for the case of various buffer layer doping concentrations. A drift region high-level lifetime of 0.6 μs and buffer layer thickness of 5 μm was assumed here. It can be observed that the carrier concentration falls below the drift region doping level of
2 × 10^{14} \text{ cm}^{-3} on the emitter side when the buffer layer doping level exceeds 2 × 10^{17} \text{ cm}^{-3}. This indicates that an increase in the on-state voltage drop can be expected for this IGBT structure when the buffer layer doping level exceeds 2 × 10^{17} \text{ cm}^{-3}. The on-state voltage drop for the 15-kV asymmetric IGBT structure obtained by using analytical model is provided in Fig. 3.65 as a function of buffer layer doping level. From the various components of the on-state voltage drop in the figure, it is clear that the voltage drop in the drift region increases rapidly once the buffer layer doping level exceeds 2 × 10^{17} \text{ cm}^{-3}.

The on-state voltage drop for the 15-kV asymmetric IGBT structure at an on-state current density of 25 A/cm² obtained by using analytical model is provided in Fig. 3.66 as a function of buffer layer doping level for various high-level lifetime values. It can be observed that the buffer layer doping concentration at which the on-state voltage drop increases rapidly becomes smaller when the high-level lifetime is reduced. It is therefore necessary to optimize these parameters together when designing the asymmetric SiC IGBT structure.

The SiC asymmetric IGBT structure can be optimized by altering the thickness of the buffer layer as a design parameter. This is illustrated for the case of the 15-kV structure in Fig. 3.67 where the carrier distribution at an on-state current density of 25 A/cm² is shown with buffer layer thickness ranging from 1 to 15 μm. A buffer layer doping level of 1 × 10^{17} \text{ cm}^{-3} and drift region high-level lifetime of 0.6 \mu s was used in all these cases. It can be observed that the injected free carrier concentration falls below the doping concentration of the drift region when the buffer layer

FIGURE 3.63
On-state voltage drop components for the SiC 15-kV asymmetric IGBT structure: lifetime dependence.
FIGURE 3.64
Carrier distribution in the 15-kV n-channel asymmetric SiC IGBT structure: buffer layer doping dependence.

FIGURE 3.65
On-state voltage drop components for the SiC 15-kV asymmetric IGBT structure: buffer layer doping dependence.
3.5 Silicon Carbide IGBT Structures

**FIGURE 3.66**
On-state voltage drop for the SiC 15-kV asymmetric IGBT structure: buffer layer doping dependence.

**FIGURE 3.67**
Carrier distribution in the 15-kV n-channel asymmetric SiC IGBT structure: buffer layer thickness dependence.
thickness is increased beyond 5 \( \mu m \). This indicates that a strong increase in the on-state voltage drop will be observed for larger values of the buffer layer thickness. This can be seen in Fig. 3.68 where the on-state voltage drop for the 15-kV asymmetric IGBT structure at an on-state current density of 25 A/cm\(^2\) obtained by using analytical model is provided as a function of buffer layer thickness for various high-level lifetime values. The voltage drop across the drift region begins to increase rapidly once the buffer layer thickness exceeds 5 \( \mu m \) resulting in a large on-state voltage drop for the IGBT. This behavior has been experimentally observed in SiC IGBTs fabricated with 2 and 10 \( \mu m \) thick buffer layers [35].

### 3.5.4 TURN-OFF CHARACTERISTICS

The asymmetric SiC IGBT structure can be expected to switch in a manner similar to that shown earlier for the silicon asymmetric IGBT structure. The hole concentration in the drift region during the voltage rise-time in the case of the silicon device becomes larger than the doping concentration in the drift region due to the low drift region doping level. Consequently, the space-charge region extends through most of the drift region but does not reach-through to the \(N\)-buffer layer at the end of the voltage rise-time. In contrast, the hole concentration in the space-charge region during the voltage rise-time for the asymmetric SiC IGBT structure is much smaller than the doping concentration of the drift region due to its high drift region doping
level and its smaller on-state current density. Consequently, the space-charge region reaches through to the buffer layer when the collector bias is well below the collector supply voltage during the voltage rise-time. When the space-charge region reaches through to the buffer layer, the electric field in the \(N\)-base region takes a trapezoidal shape allowing the collector voltage to rise at a much more rapid rate until it reaches the supply voltage.

The analysis of the turn-off waveform for the collector voltage transient for the asymmetric SiC IGBT structure can be performed by using the charge control principle as described in Section 3.2.4 for the silicon device. However, due to the lower lifetime values for SiC devices, the on-state carrier distribution profile cannot be assumed to be linear [12]. Using the on-state carrier distribution given by Eqn (3.54), the concentration of holes at the edge of the space-charge region \(p_e\) during the turn-off process is given by:

\[
p_e(t) = p(W_{NB+}) \frac{\sinh[W_{SC}(t)/L_a]}{\sinh[(W_N + W_{NB})/L_a]} \quad (3.91)
\]

Since the charge removed by the expansion of the space-charge layer must equal the charge removed due to collector current flow:

\[
J_{C,ON} = qp_e(t) \frac{dW_{SC}(t)}{dt} = qp(W_{NB+}) \frac{\sinh[W_{SC}(t)/L_a]}{\sinh[(W_N + W_{NB})/L_a]} \frac{dW_{SC}(t)}{dt} \quad (3.92)
\]

The solution for the evolution of the space-charge region width with time is obtained by integrating this equation:

\[
W_{SC}(t) = L_a a \cosh \left\{ \frac{J_{C,ON} \sinh[(W_N + W_{NBL})/L_a]}{qL_ap(W_{NB+})} t + \cosh \left[ W_{SC}(0)/L_a \right] \right\} \quad (3.93)
\]

The rate of change in the collector voltage supported by the asymmetric SiC IGBT structure can be obtained using:

\[
V_C(t) = \frac{q(N_D + p_{SC})W_{SC}^2(t)}{2\varepsilon_S} \quad (3.94)
\]

with the hole concentration in the space-charge layer is given by Eqn (3.64). In the case of SiC IGBTs designed with drift regions as described in Section 3.4.2, the collector voltage increases until the space-charge region reaches through the \(N\)-base region. The reach-through voltage is given by:

\[
V_{RT}(J_{C,ON}) = \frac{q(N_D + p_{SC})W_N^2}{2\varepsilon_S} \quad (3.95)
\]

Based upon a saturated velocity of \(8.6 \times 10^6\) cm/s for holes in SiC, the hole concentration in the space-charge region \(p_{SC}\) computed by using Eqn (3.64) is
1.8 \times 10^{13} \text{ cm}^{-3} \text{ at an on-state current density of } 25 \text{ A/cm}^2. \text{ In the case of the 15-kV asymmetric SiC IGBT structure with an } N\text{-base width of } 140 \text{ \textmu m and doping concentration of } 2.0 \times 10^{14} \text{ cm}^{-3}, \text{ the reach-through voltage is found to be } 3980 \text{ V after including the above concentration of holes in the space-charge region. The time at which reach-through of the space-charge region occurs can be obtained from Eqn (3.93) by setting the space-charge region width equal to the width of the } N\text{-base region:}

\begin{equation}
t_{RT} = \frac{qL_a p(W_{NB} + )}{J_{C,ON}} \left\{ \frac{\cosh[W_N/L_a] - \cosh[W_{SC}(0)/L_a]}{\sinh[(W_N + W_{NB})/L_a]} \right\}
\end{equation}

All the stored charge in the } N\text{-base region is removed by the voltage transient when the space-charge region reaches through the } N\text{-base region leaving substantial stored charge in the } N\text{-buffer layer. When the space-charge region reaches the edge of the } N\text{-buffer layer, the hole concentration at the buffer layer at this point becomes equal to the hole concentration (} p_{SC} \text{) inside the space-charge region, which is close to zero. Since the collector current density is held fixed during the voltage rise-time, the hole concentration in the } N\text{-buffer layer at junction (} J_1 \text{) changes abruptly when reach-through occurs. The distribution of holes in the } N\text{-buffer layer is given by [12]:}

\begin{equation}
p(y) = \frac{J_{C,ON} L_{pNB}}{q D_{pNB}} \left\{ \frac{\sinh[(W_{NBL} - y)/L_{pNB}]}{\cosh(W_{NBL}/L_{pNB})} \right\}
\end{equation}

During the next phase of the voltage rise-time, the electric field in the } N\text{-base region increases with a punch-through distribution because of the high doping concentration of the } N\text{-buffer layer. A depletion region is formed in the } N\text{-buffer layer by a displacement current flow toward the collector contact. The collector voltage waveform after reach-through is given by [12]:}

\begin{equation}
V_C(t) = V_{RT}(J_{C,ON}) + \frac{J_{C,ON}}{C_{SCR}} \left[ 1 - \frac{1}{\cosh(W_{NBL}/L_{pNB})} \right] t
\end{equation}

The end of the voltage rise-time is defined by the collector voltage becoming equal to the collector supply voltage (} V_{CS} \text{). The collector voltage rise-time is given by [12]:}

\begin{equation}
t_V = t_{RT} + \frac{\epsilon_S}{J_{C,ON} W_N} \left[ \frac{\cosh(W_{NBL}/L_{pNB})}{\cosh(W_{NBL}/L_{pNB}) - 1} \right] [V_{CS} - V_{RT}(J_{C,ON})]
\end{equation}

After the collector voltage transient, there is stored charge in the } N\text{-buffer layer which decays by recombination under low-level injection conditions. The collector current transient is described by:}

\begin{equation}
J_C(t) = J_{C,ONE} e^{-t/t_{BL}}
\end{equation}

where } t_{BL} \text{ is the low-level lifetime in the } N\text{-buffer layer. This lifetime scales with the lifetime in the drift region.}
In the case of the 15-kV asymmetric SiC n-channel IGBT structure with an $N$-base region width of 140 $\mu$m and doping concentration of $2 \times 10^{14}$ cm$^{-3}$; $N$-buffer layer doping concentration of $1 \times 10^{17}$ cm$^{-3}$ and thickness of 5 $\mu$m; and $P^+$ collector region doping concentration of $1 \times 10^{19}$ cm$^{-3}$, the collector voltage and current waveforms predicted by the above analytical model are shown in Fig. 3.69 for three high-level lifetime values. A collector supply voltage of 10,000 V and on-state collector current density of 25 A/cm$^2$ was assumed in this example. It can be observed that the collector voltage increases in a non-linear manner until a reach-through voltage of 3980 V independent of the lifetime. The collector voltage then increases linearly with a high $[dV/dt]$. After the end of the collector voltage transient, the collector current decreases exponentially to zero at a faster rate when the lifetime is reduced.

### 3.5.5 Switching Energy Loss Per Cycle

The turn-off losses in the IGBT during each cycle are associated with the voltage rise-time interval and the current fall-time interval. Due to the approximately linear increase in collector voltage, the energy loss during voltage rise-time interval until reach-through can be computed using:

$$E_{OFF,V1} = \frac{1}{2} J_{C,ON} V_{RT} t_{RT}$$

(3.101)
Since the collector voltage increases very rapidly to the supply voltage after reach-through, the energy loss for during this time can be neglected. The energy loss during the collector current fall-time interval can be computed using:

$$E_{OFF,I} = J_{C,ON} V_{C,STBL}$$

because of the exponential fall in collector current. The total energy loss per cycle is the sum of these two terms. These energy losses per cycle can be used to create a trade-off curve between on-state voltage drop and switching loss. These trade-off curves are compared with an optimized IGBT design later in the chapter. The energy losses for the optimized IGBT structure are also given by the same equations with the reach-through voltage being equal to the supply voltage.

### 3.6 OPTIMUM SiC ASYMMETRIC IGBT STRUCTURE

An abrupt increase in the collector voltage is observed for the SiC IGBT structure described in the previous section due to punch-through of the space-charge region. This behavior is undesirable in applications for IGBTs. It is possible to avoid this problem by re-engineering the drift region thickness and doping to obtain the needed forward blocking capability while allowing the space-charge region to punch-through to the buffer layer when the collector voltage reaches the supply voltage [12]. In other words, the reach-through voltage is made equal to the collector supply voltage in this design of the asymmetric IGBT structure.

#### 3.6.1 OPTIMUM STRUCTURE DESIGN

The reach-through voltage is a function of the width and the doping concentration of the drift region, as well as the on-state current density through the hole concentration in the space-charge region. Although Eqn (3.95) indicates that the reach-through voltage can be increased by solely increasing the doping concentration of the $N$-base region, this approach results in a reduction of the blocking voltage. In the case of the 15-kV SiC asymmetric IGBT device, the width and the doping concentration of the $N$-base region must be optimized together to simultaneously obtain the desired open-base breakdown voltage of 16.5 kV and a reach-through voltage equal to a collector supply voltage of 10 kV.

The possible combinations of the thickness and doping concentrations of the $N$-base region are shown in Fig. 3.70 to achieve a blocking voltage of 16.5-kV based upon using a low-level lifetime of 0.5 $\mu$s in the drift region. An $N$-buffer layer doping concentration of $1 \times 10^{17}$ cm$^{-3}$ and thickness of 5 $\mu$m was assumed here. The reach-through voltage can be computed by using Eqn (3.95) for each combination of the doping concentration and thickness of the drift region in Fig. 3.70. These reach-through voltages are plotted in Fig. 3.71 as a function of the drift region doping concentration. It can be seen that a reach-through voltage of 10 kV is obtained for a drift region doping concentration is $4.8 \times 10^{14}$ cm$^{-3}$. From
3.6 Optimum SiC ASYMMETRIC IGBT STRUCTURE

**FIGURE 3.70**
Optimization of the drift region width for the 15-kV asymmetric 4H-SiC $n$-channel IGBT structure.

**FIGURE 3.71**
Reach-through voltages for the 15-kV asymmetric 4H-SiC $n$-channel IGBT structure.
Fig. 3.70, an open-base breakdown voltage of 16.5 kV is obtained for this drift region doping concentration for a drift region thickness of 147 μm.

### 3.6.2 ON-STATE VOLTAGE DROP

The on-state voltage drop for the optimized SiC asymmetric IGBT structure can be computed using the analytical model given in the previous section with the optimum thickness of 147 μm for the drift region with a doping concentration of $4.8 \times 10^{14}$ cm$^{-3}$. The variation of the on-state voltage drop (at an on-state current density of 25 A/cm$^2$) with high-level lifetime in the drift region is shown in Fig. 3.72 for the case of a buffer layer doping concentration of $1 \times 10^{17}$ cm$^{-3}$ and thickness of 5 μm. The various components of the on-state voltage are also provided in the figure. It can be observed that the voltage drop in the drift region increases rapidly when the high-level lifetime is reduced below 0.6 μs. The on-state voltage drop for the optimum structure is slightly larger than that of the structure in the previous section at low values for the lifetime because of its larger drift region width.

The on-state voltage drop for the 15-kV optimum asymmetric IGBT structure obtained by using analytical model is shown in Fig. 3.73 as a function of buffer layer doping concentration. A high-level lifetime of 1 μs was used for this example with a buffer layer thickness of 5 μm. The various components of the on-state voltage drop are also included in the figure. The voltage drop across the drift region increases rapidly once the buffer layer doping level exceeds $2 \times 10^{17}$ cm$^{-3}$. The on-state voltage drop components for the optimum SiC 15-kV asymmetric IGBT structure: lifetime dependence.
voltage drop is larger for the optimum structure in comparison with the structure in
the previous section. For instance, at a buffer layer doping concentration of
$6 \times 10^{17}$ cm$^{-3}$, the on-state voltage drop for the optimum structure is 10% larger
than for the structure in the previous section.

3.6.3 TURN-OFF CHARACTERISTICS

In the optimum structure, the collector voltage increases monotonically to the col-
clector supply voltage followed by the collector current decaying exponentially to
zero by the recombination of holes in the $N$-buffer layer. The rise in the collector
voltage is described by the physics described in the previous section prior to
punch-through of the space-charge region. Consequently, the time at which the col-
clector voltage transient is completed can be obtained using Eqn (3.96). The current
fall occurs with the physics that governs the recombination of holes in the buffer
layer as discussed in the previous section. The on-state carrier distributions within
the optimum structure are similar to that within the conventional structure shown
in the previous section.

The collector voltage and current waveforms predicted by the above analytical
model are provided in Fig. 3.74 for various values of the lifetime in the drift region
for the case of the optimum 15-kV SiC asymmetric $n$-channel IGBT structure with
an $N$-base region width of 147 $\mu$m and doping concentration of $4.8 \times 10^{14}$ cm$^{-3}$. An
on-state collector current density of 25 A/cm$^2$ was used in this example. It can be
observed that the collector voltage increases monotonically until the reach-through time ($t_{RT}$) where it becomes equal to the collector supply voltage of 10,000 V. Consequently, there is no high $dV/dt$ during the collector voltage transient. The collector current then decays exponentially to zero with the time constant determined by the lifetime in the buffer layer. In the case of this optimum IGBT structure, the time taken for the collector voltage to rise to the supply voltage is larger than for the structure discussed in the previous section (see Fig. 3.69). Consequently, the elimination of the high $dV/dt$ during turn-off must be traded-off against larger switching losses.

The turn-off behavior for the optimum SiC asymmetric IGBT structure can also be controlled by changing the doping concentration and thickness in the buffer layer. This can be demonstrated using the example of the 15-kV SiC asymmetric optimum $n$-channel IGBT structure with an $N$-base region width of 147 $\mu$m and doping concentration of $4.8 \times 10^{14}$ cm$^{-3}$. The impact of changing the buffer layer doping concentration is provided in Fig. 3.75 for the optimum 15-kV SiC asymmetric IGBT structure with buffer layer thickness of 5 $\mu$m and high-level lifetime of 1 $\mu$s. A faster rise of the collector voltage is observed with increasing buffer layer doping concentration. This is due to the reduction of the injected carrier concentration in the drift region. The collector current also turns off faster with increasing buffer doping concentration but this is due to reduction of the buffer layer lifetime.

The impact of changing the buffer layer thickness is provided in Fig. 3.76 for the optimum 15-kV SiC asymmetric IGBT structure with buffer layer doping concentration.
FIGURE 3.75
Waveforms for the collector current and voltage for the optimum 15-kV SiC asymmetric n-channel IGBT structure during inductive load turn-off: buffer layer doping dependence.

FIGURE 3.76
Waveforms for the collector current and voltage for the optimum 15-kV SiC asymmetric n-channel IGBT structure during inductive load turn-off: buffer layer thickness dependence.
concentration of $5 \times 10^{16} \text{ cm}^{-3}$ and high-level lifetime of 1 µs. A faster turn-off occurs for the collector voltage with increasing buffer layer thickness due to the reduction of the injected carrier concentration in the drift region. However, the collector current fall-time does not change because the lifetime in the buffer layer is the same for all three cases.

### 3.6.4 POWER LOSS TRADE-OFF CURVES

As mentioned in the previous sections, the IGBT structure must be optimized by trading off the on-state voltage power loss and the switching power loss. This can be performed by making a trade-off curve between on-state voltage drop and the energy loss per switching cycle. The trade-off curves for the conventional and optimum SiC 15-kV asymmetric $n$-channel 4H-SiC IGBT structures obtained by varying the lifetime in the $N$-base region are provided in Fig. 3.77. Devices used in lower frequency circuits would be chosen from the left-hand side of the trade-off curve while devices used in higher frequency circuits would be chosen from the right-hand side of the trade-off curve. The trade-off curve for the optimum structure is worse than that for the conventional structure due to its larger on-state voltage drop and switching losses. It can be concluded that the elimination of the high $[dV/dt]$ during turn-off is obtained at the expense of higher power losses.

The trade-off curve for power losses in the 15-kV SiC asymmetric IGBT can also be performed by varying the buffer layer doping concentration. This is demonstrated

![Image](image.png)

**FIGURE 3.77**
Trade-off curves for the 15-kV asymmetric $n$-channel 4H-SiC IGBT structures: lifetime dependence.
in Fig. 3.78 for the optimum structure with a drift region thickness of 147 μm and doping concentration of $4 \times 10^{14}$ cm$^{-3}$. Two cases for the high-level lifetime in the drift region are considered in this figure. It can be observed that the trade-off curve is better for the case of a larger lifetime in the drift region. These structures require higher doping levels in the buffer layer to achieve the same turn-off losses.

### 3.6.5 MAXIMUM OPERATING FREQUENCY

The power dissipation during operation of the 15-kV asymmetric $n$-channel 4H-SiC IGBT structures can be obtained by using:

$$ P_{D,TOTAL} = \delta P_{D,ON} + E_{OFF}f $$

(3.103)

where $\delta$ is the duty cycle and $f$ is the switching frequency. The maximum operating frequency is limited by the power dissipation reaching a value decided by the packaging and heat sink. The maximum operating frequency obtained for the conventional and optimum structures is shown in Fig. 3.79 using a maximum total power dissipation of 200 W/cm$^2$. It can be concluded that the maximum operating frequency for the optimum structure is much lower than that for the conventional structure. Consequently, the elimination of the high $[dV/dt]$ during the collector voltage transient is obtained at a significant disadvantage in terms of the highest operating frequency.
3.7 SUMMARY

Although many structural variations of the IGBT have been proposed since its first introduction in the early 1980s, they can be broadly classified into symmetric blocking and asymmetric blocking devices. In this chapter, it is demonstrated that the design of these structures begins by defining the parameters of the drift region to enable the device to support the desired voltage in the blocking mode. The thickness and doping concentration of the drift region of the IGBT is determined by open-base transistor breakdown physics. For the symmetric blocking device structure, a minimum drift region thickness occurs at an optimum doping concentration for the drift region. This produces the best on-state voltage drop and switching energy loss. For the asymmetric blocking device, the drift region thickness can be minimized by proper choice of not only the drift region doping concentration but also the doping and thickness of the buffer layer. The trade-off curve between the on-state voltage drop and the switching energy loss per cycle can be optimized by adjusting the buffer layer properties and the lifetime in the drift region. This has been demonstrated by using the example of a 3000-V silicon device structure.

This chapter has also provided a review of the design of the SiC IGBT structure. Although the physics of operation of the SiC devices is similar to that of the silicon devices, the conventional approach to the design that is suitable for silicon structures produces a very high \([dV/dt]\) during the turn-off transient. It has been demonstrated that an optimum SiC device structure can be created without this high \([dV/dt]\) problem by re-engineering the drift region to make the reach-through voltage equal to the collector supply voltage. However, the optimum SiC device structure is shown to

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**FIGURE 3.79**

Maximum operating frequency for the 15-kV asymmetric \(n\)-channel 4H-SiC IGBT structures.
have a significantly worse trade-off curve between on-state voltage drop and energy loss per switching cycle.

REFERENCES