$$\gamma_{\mathrm{Sn}} = \frac{\sqrt{N_{\mathrm{i}}^2 + N_{\mathrm{i}}(1 - |\Gamma_{\mathrm{on}}|^2)}}{1 + N_{\mathrm{i}}} \tag{14.5.8}$$

Notwithstanding our distinction between noise factor and noise figure, the constant noise factor circles defined here are often referred to as *constant noise figure circles*, which reflects the fact that they are often labeled with the noise figure value in dB.

We will now illustrate the use of constant noise figure circles with an example.

**Example 14.1** (Noise figure circles).

**Problem.** Draw constant noise figure circles for $F = 1.4$ dB, $F = 2$ dB, and $F = 3$ dB on the source plane for the Avago ATF-34143 Low-Noise HEMT operating at 10 GHz, and hence, or otherwise, determine the lowest possible noise figure commensurate with the maximum gain available from this device. The $S$-parameters and noise parameters of the device with bias conditions $V_{\mathrm{DS}} = 3$ V, $I_{\mathrm{DS}} = 40$ mA are as follows:

$S$-parameters:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.760\angle 28 & 0.144\angle -84 \\ 1.647\angle -84 & 0.410\angle 23 \end{bmatrix}$$

Noise parameters:

$$\begin{aligned} F_{\mathrm{min}} &= 1.22 \text{ dB} \\ \Gamma_{\mathrm{on}} &= 0.61\angle -39^\circ \\ R_{\mathrm{n}} &= 25\ \Omega \end{aligned}$$

**Solution.** First, we need to investigate the stability of the device, for which we will use the Edwards-Sinsky stability criteria defined by equations (7.4.36) and (7.4.37), that is,

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} = \frac{0.4224}{0.3134} = 1.1887$$

$$\mu_2 = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} = \frac{0.8319}{0.8246} = 1.0435$$

Since both $\mu_1$ and $\mu_2$ are greater than 1 we conclude that the device is unconditionally stable, so we are free to choose any terminating impedances lying within the $|\Gamma| = 1$ boundary of the source and load plane Smith Charts. Maximum available gain (MAG) occurs when the source and load are simultaneously conjugately matched. The necessary terminating reflection coefficients are determined using equations (14.4.10) and (14.4.11) as follows:

$$\Gamma_{\mathrm{ms}} = C_1^* \left[ \frac{B_1 + \sqrt{B_1^2 - 4|C_1|^2}}{2|C_1|^2} \right]$$

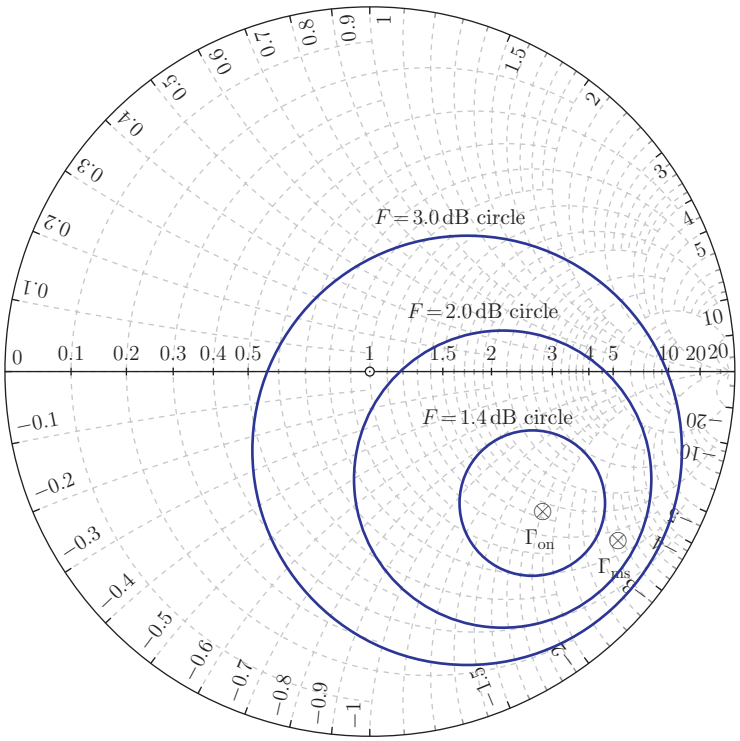


**FIGURE 14.6**

Constant noise figure circles for Avago ATF-34143 at 10 GHz ($V_{DS} = 3$ V, $I_{DS} = 40$ mA).

noise figure and gain, as these optima generally do not occur with the same source termination. Furthermore, the active device may be potentially unstable, which will further restrict the choice of source and load termination. We can illustrate this rather more complicated scenario by means of another example, as follows.

**Example 14.2** (Low-noise design for specified gain).

**Problem.** You are required to design an 18 GHz low-noise amplifier having a gain of at least 10 dB and a noise figure of less than 2 dB, using the BFU730F Silicon-Germanium BJT from NXP. The *S*-parameters and noise parameters of the device with bias conditions $V_C = 2.0$ V, $I_C = 10$ mA are as follows.

*S*-parameters:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.691\angle 63^\circ & 0.178\angle -20^\circ \\ 2.108\angle -55^\circ & 0.218\angle 97^\circ \end{bmatrix}$$

Noise parameters:

$$F_{\min} = 1.79 \text{ dB}$$
$$\Gamma_{\text{on}} = 0.667\angle 307^\circ$$
$$R_{\text{n}} = 28.6\ \Omega$$

**Solution.** First, we need to investigate the stability of the device, for which we will use the Edwards-Sinsky stability criteria of equations (7.4.36) and (7.4.37), that is,

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} = \frac{0.4224}{0.3134} = 0.885$$

$$\mu_2 = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} = \frac{0.8319}{0.8246} = 0.962$$

Since both $\mu_1$ and $\mu_2$ are less than 1 we conclude that the device is potentially unstable. We therefore need to plot stability circles in order to determine the acceptable range of source terminations. Since we need to focus on matching the input port to achieve the desired noise specification, we first use equations (7.4.14) and (7.4.15) to calculate the center and radius of the source plane stability circle, as follows:

$$C_{\text{SS}} = \frac{C_1^*}{|S_{11}|^2 - |\Delta|^2} = \frac{0.6149\angle -62^\circ}{0.2492} = 2.4680\angle -69^\circ$$

$$r_{\text{SS}} = \left|\frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2}\right| = \frac{0.3752}{0.2492} = 1.5060$$

Once again, we calculate the parameter $N_{\text{i}}$, as defined by equation (14.5.3), for various values of noise figure circle (say, $F = 2$ dB, $F = 3$ dB, and $F = 5$ dB). We then calculate the respective noise figure circle centers and radii using equations (14.5.7) and (14.5.8). The resulting calculations are summarized in the following table.

| $F$ (dB) | $N_{\text{i}}$ | $\lvert C_{\text{Sn}}\rvert$ | $\angle C_{\text{Sn}}$ | $\gamma_{\text{Sn}}$ |
|---|---|---|---|---|
| 2 | 0.0735 | 0.6213 | −53° | 0.2002 |
| 3 | 0.4766 | 0.4517 | −53° | 0.4749 |
| 5 | 1.6231 | 0.2543 | −53° | 0.7168 |

The above noise figure circles are plotted on the source plane Smith Chart, together with the stability circle as shown in Figure 14.7.

We now check the gain available from the device when terminated for minimum noise figure, that is, when the source termination is $\Gamma_{\text{on}} = 0.667\angle 307^\circ$. For this we use equation (7.5.13) for available power gain:

$$C_{S_m} = \frac{M|1+\Gamma_{on}|^2 C_1^* + 4r_n|S_{21}|^2\Gamma_{on}}{M|1+\Gamma_{on}|^2(|S_{21}|^2+|S_{11}|^2-|\Delta|^2)-|S_{21}|^2(|1+\Gamma_{on}|^2(F_{min}-1)-4r_n)} \tag{14.6.14}$$

and the radius is given by:

$$\gamma_{S_m} = \sqrt{\frac{M|1+\Gamma_{on}|^2(1-|S_{22}|^2-|S_{21}|^2)+|S_{21}|^2[|1+\Gamma_{on}|^2(F_{min}-1)+4r_n|\Gamma_{on}|^2]}{M|1+\Gamma_{on}|^2(|\Delta|^2-|S_{21}|^2-|S_{11}|^2)+|S_{21}|^2(|1+\Gamma_{on}|^2(F_{min}-1)-4r_n)}+|C_{S_m}|^2} \tag{14.6.15}$$

We can determine the value of the minimum noise measure obtainable with a given device by considering the noise measure circle of zero radius. This means finding a value of $M$ that makes $\gamma_{Sm}$ in equation (14.6.15) equal to zero. This can be done by trial and error, although closed form solutions have also been proposed [27,28].

The source reflection coefficient which gives rise to $M_{min}$ is the center of the $M_{min}$ noise measure circle. Once the value of $M_{min}$ has been determined, the value of $\Gamma_{om}$ can therefore be determined from equation (14.6.14) as:

$$\Gamma_{om} = \frac{M_{min}|1+\Gamma_{on}|^2 C_1^* + 4r_n|S_{21}|^2\Gamma_{on}}{M_{min}|1+\Gamma_{on}|^2(|S_{21}|^2+|S_{11}|^2-|\Delta|^2)-|S_{21}|^2(|1+\Gamma_{on}|^2(F_{min}-1)-4r_n)} \tag{14.6.16}$$

With the input port of the transistor terminated in $\Gamma_{om}$, we can calculate the output reflection coefficient looking into the output port of the transistor by employing equation (6.2.7), that is,

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_{om}}{1-S_{11}\Gamma_{om}} \tag{14.6.17}$$

The use of these equations is best illustrated by means of an example.

**Example 14.4** (Minimum noise measure design).

**Problem.** Design a single-stage amplifier for minimum noise measure using an NE71083 GaAs MESFET at a center frequency of 10 GHz and bias conditions $V_{ds} = 3.0$ V, $I_d = 8$ mA. The $S$-parameters of the transistor in the common source configuration were measured, with a 50 Ω reference impedance, to be as follows:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.724\angle 46^\circ & 0.716\angle -47^\circ \\ 1.303\angle -10^\circ & 0.616\angle 64^\circ \end{bmatrix} \tag{14.6.18}$$

The following noise parameters were supplied by the manufacturer of the FET:

$$F_{min} = 1.7 \text{ dB}$$
$$\Gamma_{on} = 0.620\angle 148^\circ$$
$$r_n = 12\ \Omega$$

can be approximately determined from equation (1.3.1) and typical values will be in the order of hundreds of pH. For MMICs operating at frequencies exceeding 20 GHz multiple parallel bond wires or ribbon bonding can be used to reduce the effective inductance.

Many other passive structures are found in MMICs, such as air bridges, transmission line filters, and even antennas. Recent developments have included the incorporation of microelectromechanical systems (MEMS) that are created on the same die, alongside conventional electronic devices. For a survey of MEMS and their uses in microwave systems, the interested reader is referred to Rebeiz's book [75]. A nice example of how MEMS are incorporated with an MMIC is given by Kim [76].

## 12.9 MMIC APPLICATION EXAMPLE

In this section, we will briefly describe the design and implementation of a wideband distributed amplifier (DA), operating from tens of MHz to hundreds of GHz, as a way of illustrating the capabilities of contemporary MMIC technology [9]. The DA is a particular broadband amplifier topology that will be discussed in more detail in Chapter 13.

This example uses an InP DHBT process with 250 nm emitter width and where the gain of the transistor is dependent on the number of emitter fingers and, of course, the transistor bias. The unity-gain cut-off frequency of these transistors, $f_T$, is close to 350 GHz and the maximum frequency of oscillation, $f_{max}$, is close to 650 GHz. The process is described in detail in Ref. [77].

The process has four metallization layers (M1-M4) and four dielectric layers. The dielectric consists of a 1 μm layer of the organic compound benzocyclobutene (BCB). A schematic cross-section view of the back-end is shown in Figure 12.24.

The thickness of the M1, M2, and M3 layers is $\sim 1$ μm, whereas M4 is 3 μm thick to support higher current densities. The process includes TFR and MIM capacitors. The InP substrate thickness is 100 μm. The topmost layer, M4, is utilized for signal connections and the second metal layer, M2, is used as a ground plane. This allows low inductive connections (between emitter and ground) when the transistors are used in common emitter configuration which is highly important for achieving high gain when operating up to frequencies close to the $f_{max}$ of the transistors. The first metal layer, M1, is shielded from the RF signal by M2 and can be used for DC connections without disturbing the RF signals on M4.

A photomicrograph of a three-stage DA MMIC is shown in Figure 12.25. The die size is 0.86 mm $\times$ 0.37 mm. In this circuit, each of the amplifying stages has two DHBT transistors configured as a *cascade* gain cell, that is, an input transistor in common emitter configuration, the output of which is connected to a transistor in common base configuration. The common emitter devices are visible just at the top of the "L"-shaped transmission lines and the common-base devices can be seen on the lower right of the same lines.

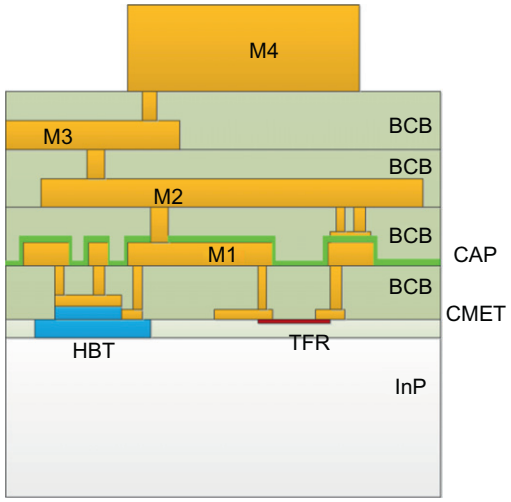


**FIGURE 12.24**

Schematic cross-section view of the multilayer interconnect back-end process.

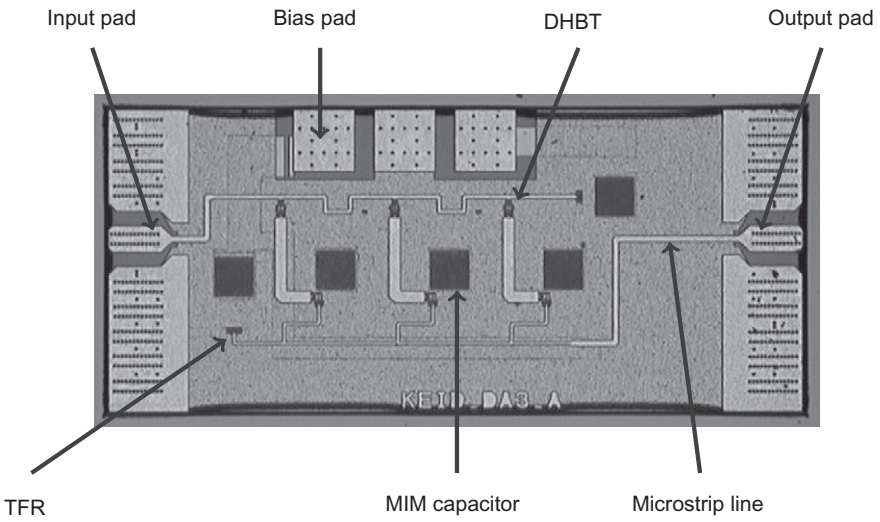


**FIGURE 12.25**

Photomicrograph of a three-stage DA MMIC. Circuit size: 0.86 mm × 0.37 mm.

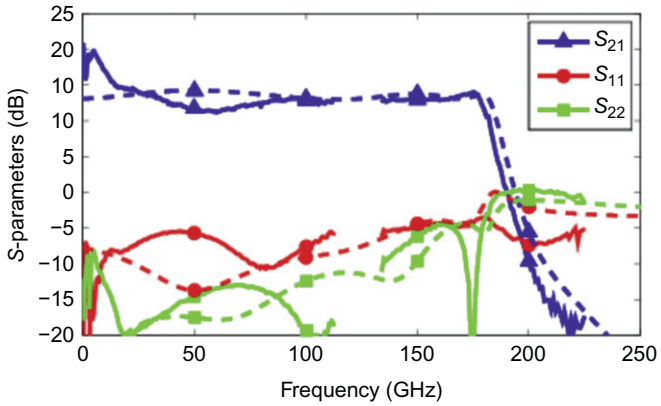


**FIGURE 12.26**

Simulated and measured frequency response of the three-stage MMIC DA in Figure 12.25.

A high impedance microstrip line ($Z_o = 70\ \Omega$) was used at the output of each gain cell to improve the bandwidth. The connections from the input transmission line to the common emitter devices were designed to be as short as possible, since any inductance here reduces the gain and the bandwidth. The two devices in each gain cell are connected with an "L"-shaped low impedance, low-loss microstrip line.

Figure 12.26 shows the measured (solid-line) and simulated (dotted-line) frequency responses of the three-stage DA MMIC shown in Figure 12.25. The amplifier demonstrates more than 10 dB gain from 70 kHz up to 180 GHz. At 180 GHz and above, the gain drops sharply. Due to the very wide bandwidths involved, the amplifier had to be measured in three separate frequency bands, using three different network analyzers:

**(i)** between 70 kHz and 115 GHz;
**(ii)** 130-220 GHz; and
**(iii)** 220-300 GHz.

Unfortunately, no measurements could be carried out between 115 and 130 GHz due to nonavailability of test equipment in this band.

The amplifier briefly described here was a member of a family of three amplifiers that were fabricated using the same process, as detailed in Ref. [9]. One of these amplifiers, at the time of publication (2014), was the widest band amplifier reported, with an average gain of 16 dB over a bandwidth of 235 GHz. Such results would have been inconceivable before the advent of the advanced microwave transistors, such as the HBT and MMIC integration technologies described in this chapter.

## 12.10 TAKEAWAYS

1. Microwave transistors may be broadly divided into two categories: the BJT and the FET. The former category includes HBT. The latter category includes HEMT.
2. Microwave transistors can be represented by their equivalent circuit models to facilitate circuit design. The component values in an equivalent circuit can be determined from measured *S*-parameters or immittance parameters on the device.
3. A transistor equivalent circuit model may be partitioned into *intrinsic* and *extrinsic* elements. The extrinsic components of BJT/HBT and MESFET/HEMT transistors with similar packaging tend to be similar.
4. The bandwidth of a transistor can be characterized in terms of its cut-off frequency, $f_T$, and its maximum frequency of oscillation, $f_{max}$. These vary by transistor type and geometry, and can be calculated based on equivalent circuit component values.
5. There are a number of different techniques for fabricating lumped elements, such as resistors, inductors, and capacitors in MMIC format. The choice of technique depends on the value required and other parameters, such as power handling requirements (in the case of resistors) or dielectric loss requirements (in the case of capacitors).

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configuration is commonly used where high bandwidth is needed as the loading of the common source with a common gate, the latter with an input resistance of $1/g_m$, removes the effect of large input capacitance due to the *Miller effect*, where the capacitance at the input of the stage appears as the gate drain capacitance multiplied by the voltage gain [19].

The final stage is a high input impedance-low output impedance common source stage, $Q_5$, with an active source load, $Q_4$. This load is a MESFET that has its gate and source terminals shorted ($V_{gs} = 0$), effectively resulting in the MESFET drain-source channel acting as an "active" resistor and designed to have an output resistance close to 50 Ω so that it is well matched to the following stages. Note that all transistors in this circuit were biased by providing voltages to their gates through large (5 kΩ) resistors so that low input noise is obtained. As this particular circuit was designed for use in optical receiver applications where the input is current generated from a photodiode, the gain is measured as the ratio of the output voltage to the input current and therefore has units of Ω, or the rather unusual unit of dB Ω, which is ohms expressed in dB. Such amplifiers are called *transimpedance* amplifiers. This particular circuit has a gain of 1000 Ω or 30 dB Ω.

The circuit shown in Figure 13.12 is an enhancement of the circuit of Figure 13.11 using shunt feedback networks around both the first and second stages. This circuit was designed to operate over a frequency range from few MHz to 3.5 GHz. This MMIC is also designed for an optical receiver application, for which it is important to have low input resistance so that the *RC* time constant of the photodiode (which is effectively a capacitive current source) together with the amplifier input resistance is minimized. This situation differs from the usual 50 Ω voltage sources encountered in most microwave circuits. The circuit of Figure 13.12 reduces the input resistance to a few ohms by replacing the common source MESFET used in Figure 13.11 by a common gate input stage. The already low input resistance of the common gate is further reduced by the 1000 Ω feedback applied and AC coupled with a 4 pF capacitor. This feedback has the dual purpose of reducing the input resistance and also extending the bandwidth. The main gain stage is the second cascade stage which also has its bandwidth extended by applying feedback. Circuits of this type require careful design as they use two feedback loops and therefore may have potential instability problems. This circuit demonstrated a 4.8 GHz bandwidth and a transimpedance gain of 180 Ω or 23 dB Ω.

Comparing the two circuits of Figures 13.11 and 13.12, we can see that, as we would expect, the effect of using two feedback loops results in extended bandwidth at the cost of a reduction in gain.

### 13.5.3 DISTRIBUTED AMPLIFIERS

Amplification from a combination of two or more active devices may be classified as either multiplicative or additive [20]. In the case of the former, the overall power gain is proportional to the product of the gains supplied by the individual stages, while in

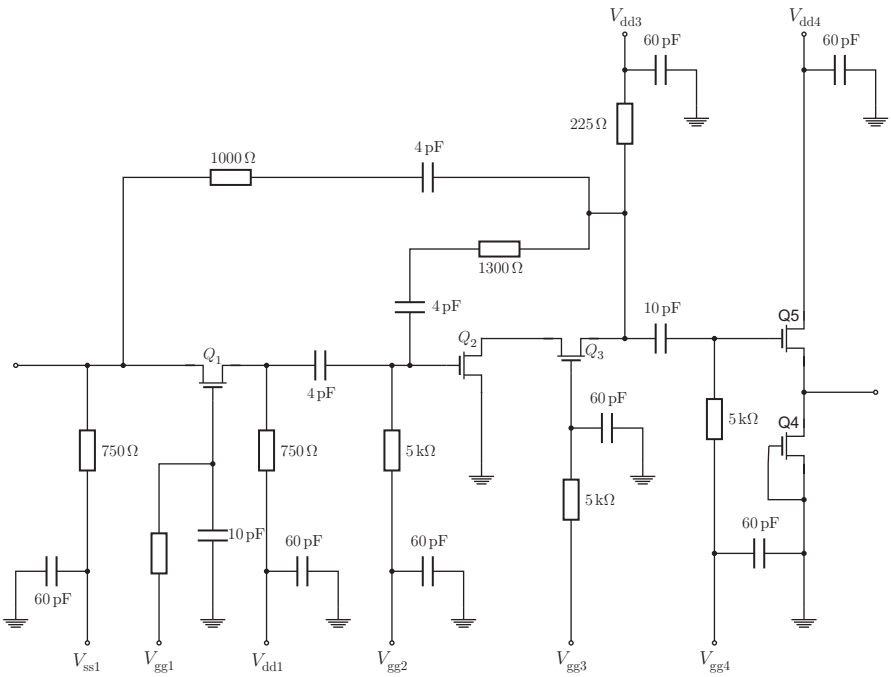


**FIGURE 13.12**

Common gate (5 Gbit $s^{-1}$) MMIC feedback amplifier.

the latter case it is proportional to the sum of the powers contributed by the individual active devices.

The vast majority of multistage amplifiers, and all those discussed in this chapter so far, make use of the multiplicative process through cascading. In this section, we will introduce an entirely different multistage amplifier architecture called the *Distributed Amplifier (DA)* [21] in which the output powers of the individual stages are combined additively. While in most practical applications this approach produces less gain per device than the multiplicative approach, it yields significant bandwidth benefits.

The concept of distributed amplification was first proposed by Percival in 1936, who introduced this novel idea in a patent specification relating to the design of thermionic valve circuits [21]. The term "distributed amplifier" was actually coined by Ginzton et al., in their 1948 paper [22] on such circuits. Prior to the advent of the transistor in 1948, vacuum tubes were employed as the active devices in DAs. One of the earliest reports of a DA implemented using transistors was made by Enloe and Rogers [23], who reported two simple DA circuits based on BJT technology.

Following the emergence of MESFET technology in the late 1960s, Jutzi published a paper in 1969 in which he gave details of a silicon MESFET-based DA with a bandwidth of 2 GHz [24], and the first GaAs MESFET-based DA, having a bandwidth of 6 GHz, was reported in 1981 [25]. That year also saw the first reported example of a DA in MMIC form [26], having a gain of 9 dB over 1-13 GHz. Subsequent years saw the emergence of monolithic DAs employing GaAs HEMTs [27] and heterojunction bipolar transistors (HBTs) [28,29]. The exceptionally wide bandwidth of DAs has resulted in their application in numerous applications requiring wideband amplification at microwave and millimeter wave frequencies [30]. Such applications include fiber optic and satellite communication systems, as well as phased array radar and broadband instrumentation.

We will proceed to describe the operation of the DA, with reference to Figure 13.13. A DA is essentially an additive amplifier, where the output currents of multiple gain stages, $A$, are superimposed constructively while ensuring that the effects of input and output shunt capacitances are not accumulated.

The basic conceptual architecture of a DA consists of a pair of transmission lines, shown as the upper and lower line in Figure 13.13. An input signal injected into the lower transmission line will propagate down the line and will arrive at the terminating resistor, $R_1$, which is a matching resistor having the same value as the line characteristic impedance, $Z_o$. As the signal propagates along the lower transmission line, the inputs of the individual gain stages are driven with a particular phase relationship to each other, determined by their position along the line. The input signal is amplified by each gain stage, and the stage outputs are combined coherently (i.e., with their phase relationships preserved) in the upper transmission line. The propagation characteristics of the upper and lower transmission lines in Figure 13.13 must be designed to be equal so as to ensure that output signals from each individual gain stage sum in phase.

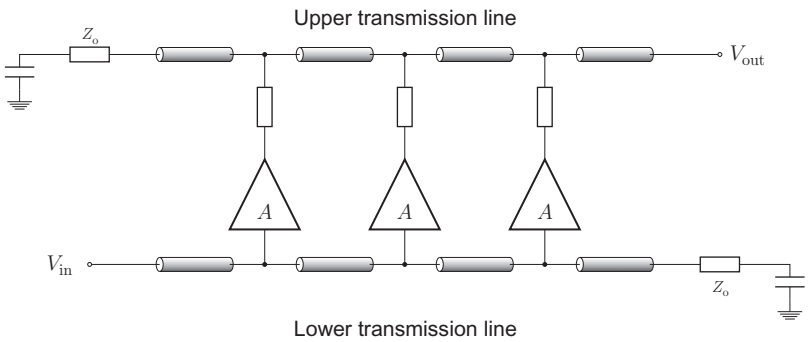


**FIGURE 13.13**

Conceptual DA architecture.

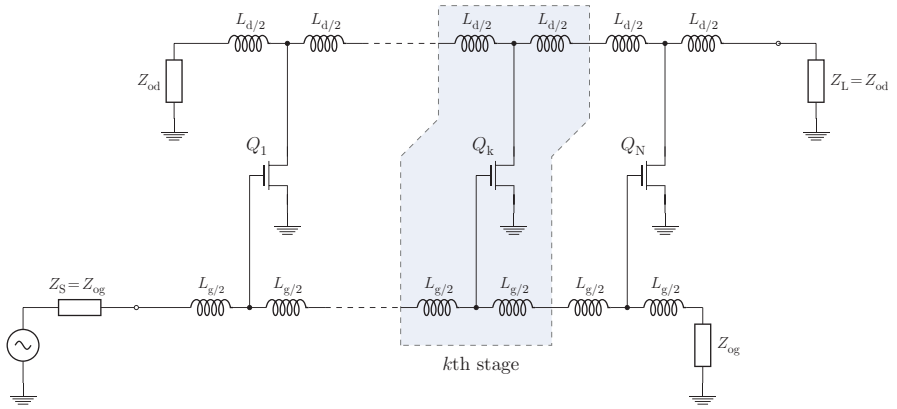


**FIGURE 13.14**

Basic AC circuit schematic of an $N$-stage MESFET DA.

The gain stages in Figure 13.13 can be implemented as single transistor amplifiers, as shown in Figure 13.14, which shows the basic AC circuit of a DA with $N$ identical transistor amplifier stages. The active devices are shown in Figure 13.14 are MESFETs or HEMTs, but the following description applies equally to bipolar transistors (BJT or HBT).

A single DA section is comprised of four inductors plus an active device as indicated in the shaded section of Figure 13.14. The simplified small signal equivalent circuit of each transistor is shown in Figure 13.15(a), and is based on the intrinsic part of the equivalent circuit in Figure 12.9 of Chapter 12, with the omission of the input resistance, $R_i$, the output drain-source resistance, $R_{ds}$, and the gate-drain feedback capacitance, $C_{gd}$. The omission of these components do not materially affect our analysis of distributed amplified operation. The important equivalent circuit parameters are $C_{gs}$, the intrinsic gate-source capacitance, and $C_{ds}$, the drain-source capacitance.

Figure 13.15(b) and (c) shows the simplified small-signal equivalent circuit models for the input and output portions of an MESFET DA, respectively. The current source in parallel with $C_{ds}$ in Figure 13.15(c) represents the intrinsic current that is generated by an MESFET through its gain mechanism. $g_m$ is the complex transconductance which, when multiplied by the input voltage $v_{gs}$ developed across $C_{gs}$, gives the value of the drain current produced internally by the MESFET. $L_g$ and $L_d$ are the total inductances present between the input base and output collector terminals of adjacent transistors, respectively.

We demonstrated in Chapter 2 that an ideal uniform lossless transmission line can be represented by an equivalent electrical model consisting of a distributed total series inductance $\Delta L$ and a distributed shunt capacitance $\Delta C$ [31], as shown in Figure 13.16. The quantities $\Delta L$ and $\Delta C$ are termed "distributed" because they

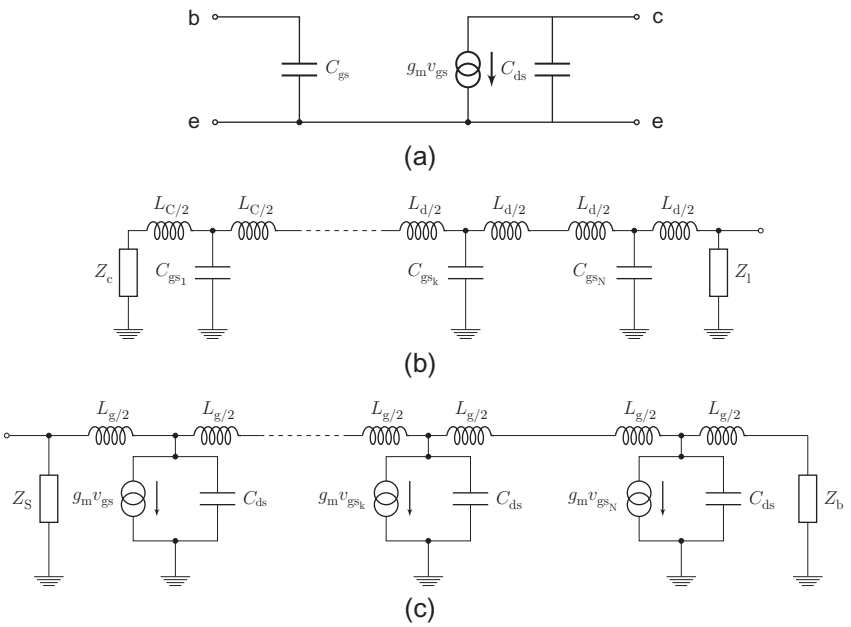


**FIGURE 13.15**

Simplified small-signal equivalent circuit models of MESFET-based DA artificial transmission lines. (a) Individual MESFET equivalent circuit. (b) Gate-line equivalent circuit. (c) Drain-line equivalent circuit.

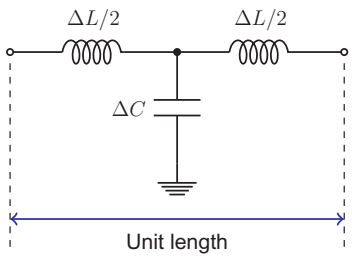


**FIGURE 13.16**

Unit length element of an ideal uniform lossless real transmission line.

are defined per unit length of transmission line. If we compare Figure 13.15 with Figure 13.16 we notice that the input and output portions of a DA each resemble the equivalent circuit model of a lossless transmission line. Consequently, a direct analogy can be established between the two circuit portions of a DA and a transmission line where the transistor parasitic capacitances, $C_\pi$ and $C_{ce}$, are

incorporated into what is, in effect, an *artificial transmission line* (ATL). A DA can essentially be viewed as a pair of transmission lines, coupled via the active devices and thus possess amplifying properties.

When field effect devices are utilized in a DA, the input and output ATLs are known as the gate-line and the drain-line, respectively. Conversely, when bipolar devices are employed, the input and output ATLs are referred to as the base line and the collector line, respectively.

An important consequence of the transistor input and output capacitances being incorporated into an ATL is that they are not lumped together at the input and output ports, as they would be if the transistors were simply connected in parallel. A parallel connection would increase the total capacitance and thereby reduce the bandwidth of the amplifier, whereas the distributed approach actually makes use of these capacitances. Consider an ideal real transmission line (RTL) that has an inherently wide bandwidth and possesses low-pass filtering characteristics. The upper bandwidth cut-off frequency of a lossless RTL is determined solely by the values of $\Delta L$ and $\Delta C$. Due to their transmission line-like nature, DAs possess the key attributes of RTLs. In particular, an ATL cut-off frequency depends only upon the amount of inductance and capacitance present per DA section and not upon the actual number of sections employed. This is in contrast to a conventional amplifier in which the upper cut-off frequency decreases with the number of cascaded gain stages.

Ideally, the gain of a DA can be made larger by increasing the number of amplifier sections, while bandwidth is preserved since it is fixed by the cut-off characteristics of the ATLs. By virtue of the independence of the amplifier properties that set bandwidth and gain, the GBP of a DA may even exceed $f_T$ of the active devices themselves.

Having ignored $R_i$ and $R_{ds}$ in the MESFET equivalent circuits, the gain of the amplifier is given by [32]:

$$G = \frac{1}{4} N^2 g_m^2 Z_{og} Z_{od} \tag{13.5.4}$$

where $N$ is the total number of stages and $Z_{og}$ and $Z_{od}$ are the characteristic impedances of the gate and drain ATLs, respectively, and are therefore the values of the terminating impedances employed in Figure 13.14. These characteristic impedances are given by:

$$Z_{og} = \sqrt{\frac{L_g}{C_{gs}}} \tag{13.5.5}$$

$$Z_{od} = \sqrt{\frac{L_d}{C_{ds}}} \tag{13.5.6}$$

Equation (13.5.4) would seem to suggest that it is possible to increase the amplifier gain by simply increasing the number of stages. The losses introduced by $R_i$ and $R_{ds}$, however, which we have ignored in this analysis so far, result in an optimum

number of stages to maximize the gain for a given active device [32]. In theory, the gain of a DA should remain flat up to the $f_T$ of the active devices, provided that the cut-off frequency of the ATLs is made much higher than the device $f_T$. The cut-off frequencies of the gate and drain ATLs are given by:

$$f_{cg} = \left( \frac{1}{\pi \sqrt{L_g C_{gs}}} \right) \tag{13.5.7}$$

$$f_{cd} = \left( \frac{1}{\pi \sqrt{L_d C_{ds}}} \right) \tag{13.5.8}$$

A consequence of the equations (13.5.5) to (13.5.8) is that once the characteristic impedance of the ATL has been chosen then the cut-off frequencies cannot be chosen independently. Up till now we have considered the use of matching networks to interconnect circuits having different characteristic impedances. In the case of DAs, which are by their nature extremely broadband, the characteristic impedance of the ATLs that make up the DA are constrained by the need to match directly to preceding and subsequent circuits.

In this chapter, we have focused on conventional and broadband amplifiers, without regard to their noise performance. Consequently we have used resistors to effect the necessary matching, such as in the case of lossy matched and DAs. The disadvantage of using resistors is that they inevitably add thermal noise. In the next chapter, we will specifically address the issue of noise in electronic circuits and low-noise amplifier design.

## 13.6 TAKEAWAYS

1. In order to obtain the optimum gain from a microwave transistor, matching networks are required at the input and output ports of the device to match the required source and load terminations to the system characteristic impedance. The source and load terminations presented to the device are constrained by requirements of gain and stability, and may be otherwise constrained (as in the case of low-noise amplifiers).
2. Single-stage transistor amplifier design can be greatly simplified by assuming that the transistor is unilateral, that is, $S_{12} = 0$. The validity of this assumption can be quantified using a parameter called the unilateral figure of merit ($U$), which can be calculated from the device $S$-parameters and is invariant under lossless, reciprocal embeddings.
3. Feedback can be used to change the $S$-parameters of a given transistor so as to simplify the amplifier design and allow more degrees of freedom. For example, we can apply shunt feedback to reduce $S_{12}$ to a minimum, allowing the unilateral assumption to be applied to the subsequent design.
4. If more gain is needed, this can be obtained by cascading single-stage amplifiers to form a multistage amplifier. This requires interstage matching networks to

ensure that the correct terminating impedances are presented to each stage, ensuring optimum power transfer between stages. The *Bode-Fano criteria* set the fundamental limits on the degree of match that can be achieved over a particular bandwidth.

5. There is an inevitable trade-off between gain and bandwidth in multistage amplifiers, but bandwidth can be optimized by the use of feedback or by such strategies as lossy interstage matching.
6. The *Distributed Amplifier (DA)* topology overcomes the limitations of conventional multistage amplifiers by adopting an additive rather than a multiplicative approach to combining the outputs of multiple stages.

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