INTRODUCTION

Wireless communication is today one of the most important ways to transport voice, video, and data using radio-frequency (RF) or microwaves. In fact, since 2002, more phone calls are made via a wireless link rather than a wired link. Even more striking, according to recent statistics on a global scale, today there are already more mobile phone subscriptions than people with access to electricity or access to safe drinking water. The modern mobile handheld terminal, the smartphone, is a clear example of it; it transports voice via a GSM, or W-CDMA cellular communication pipe and data/video can be transported via the WLAN connectivity pipe. Microwaves are typically used for satellite links to broadcast television, to enable internet for remote areas, and for private networks.

In a wireless infrastructure, wireless devices can communicate with each other or communicate with a wired network. In a cellular wireless infrastructure the communication goes first through an access point, called the base station. The mobile handheld device communicates via the base station (BTS) with another mobile device or can access the wired network. Communication takes place in the RF cellular frequency bands from 700 MHz up to 3 GHz with the upcoming LTE-A operating in even higher frequency bands between 3 and 4 GHz. Base stations communicate between themselves via a wired (optical) or again wireless link. The wireless link is very important and is referred to as the microwave backhaul of the base station. The communication happens at various microwave frequencies in the 13–40 GHz range. As base stations do have a fixed geographical position, the communication between base stations is a so-called point-to-point communication, the antennas needed for the microwave backhaul are pointed to each other (i.e. line-of-sight setting).

A satellite (wireless) infrastructure operates in a similar way, where the satellite can be considered as the base station or the access point. At the other end one finds the indoor-unit or set-top-box which is connected to the outdoor unit, the transceiver, and the dish. Most often the wireless downlink communication happens in the 10.7–12.75 GHz Ku-band, but the 18.2–22.0 GHz Ka-band is becoming popular too.
Uplink communication, that is the link from earth to satellite, takes place in the 13 GHz or 30 GHz frequency bands.

1.1 The cellular infrastructure

Mobile data traffic is expected to increase 18-fold over the next five years to 11 Exabytes per month by 2016 as a result of an ever-increasing demand for data throughput driven by widening spread of smartphones and, even faster, of tablet devices and other data-hungry mobile devices. In the meantime, wireless technologies like LTE Advanced are approaching the physical limits for achievable channel capacity because the spectrum is a limited resource. The consequence of all this is that further growth of the network capacity must come from new networks where for instance macro cells are overlaid by small cells and offload of mobile networks might take place with seamlessly integrated WiFi access points.

A macro cell base station delivers the best performance and coverage, but is very expensive to roll out. The cell radius of a macro base station is around 1–25 km and can handle more than 256 users. The average transmitted power is more than 10 W; peak power is more than 100 W. A macro base station consists of one or more reasonable-sized cabinets plus a big tower, which means that in very populated areas acquiring a site to install the macro base station might be difficult and very expensive.

The small cell can densify the macro cell network in urban areas with a lower total cost of ownership. Small cells, a collection of pico and micro cells, typically have a cell size between 200 m and 1 km and can handle up to 256 users. The average transmit power is around 5 W. However, a high-performance backhaul is mandatory for optimal performance. This backhaul can be wired or wireless. The macro cells and small cells together should deliver a high-quality (e.g. best coverage and capacity) user experience for voice and data.

The addition of WiFi access points should improve the capacity in high-traffic areas and “hot spots” and is mainly data centric.

The backhaul is a key element for high-performance cellular networks. The majority of the microwave, wireless, links use the spectrum between 6 and 38 GHz and offer capacities up to 400 Mbps with 56 MHz channel bandwidth and 256 QAM constellation. The main challenge in the microwave backhaul is the required line-of-sight (LOS) and strict alignment between the two end points. The requirement of LOS can be relaxed by the introduction of beam forming techniques and/or advanced MIMO techniques.

1.2 The satellite infrastructure

The microwave satellite market is a mass market with over 80 million outdoor units in 2012. The majority of the outdoor units are for satellite TV reception in the Ku-band. This is a mainly one-way communication pipe with the satellite. A smaller market is the two-way communication pipe for applications like credit card data, internet in remote areas, maritime communication, and private networks (e.g. CNN).
This very-small-aperture-terminal (VSAT) communication uses data rates up to 4 Mbps. The name VSAT depicts the size of the antenna, a dish antenna that is smaller than 3 m.

The low-noise block (LNB) outdoor unit is the receiver converting the received satellite signals in the Ku-band down to the L-band (950–2100 MHz). The LNB is connected via a coax cable to the set-top-box in the house, where the customer can select the TV channel. The set-top-box will power the LNB via the coax cable. Consequently, as the set-top-box can only deliver a certain amount of power, the power consumption of the LNB is a critical design parameter.

1.3 Challenges

Wireless infrastructure, be it cellular or satellite, is a more professional market segment rather than consumer market segment. Consequently, the market is traditionally driven by performance demand rather than by cost. A typical RF card in a base station or a low-noise block down converter unit in a satellite receiver is mainly based on discrete III–V compound technology components. They deliver the required performance, while the associated cost and power consumption is a lesser issue. But this landscape is changing. Mobile phone operators see their energy bills exploding while they are expanding the capacity of their cellular infrastructure. And as the expansion is taking place in dense areas like shopping malls, the installed access point should be small in size too. If satellite communication should become available in developing areas such as India and South America, a price reduction would be needed.

Consequently, there is a need to move away from III–V compound technologies toward silicon-based solutions, which inherently can provide cost reduction and power dissipation reduction, similar to what has been observed in mobile handheld devices in the past. However, the required performance, more easily delivered by GaAs-like technologies, should not be compromised. This is a challenge for silicon-based technologies where the active devices inherently have poorer performance. The RF radio especially will face challenges from this technology change.

This book will address the various issues related to the transition from III–V compound technology toward silicon-based solutions for RF radios in wireless infrastructure.

On the other hand, the data converters (ADCs and DACs) in the same signal chain have already seen a substantial shift from a mix of BiCMOS and CMOS designs to a near monopoly of CMOS data converters in the most recent designs. Some of the driving forces behind this technology shift follow.

First of all, starting from 0.18 μm and even more with finer-lithography CMOS processes, the transition frequency, \( f_T \), of MOS devices has become very competitive with the one of many of the bipolar devices available with some of the mainstream BiCMOS processes and for a comparable price. Moreover, both the active and passive device matching have been steadily improving with CMOS scaling. Combining that with the far greater level of integration achievable in CMOS makes nanometer-scale CMOS processes far more attractive than BiCMOS alternatives in designs with moderate resolution (10–16 bits) and a high sample rate (100 MSPS–1 GSPS and beyond) that are needed for wireless infrastructure.
One of the many design challenges associated with this process technology shift is represented by the lower and lower power supply usable with scaled CMOS processes. Specifically, 3.3 V and 5 V analog supplies, which were common for older BiCMOS data converters, have been replaced with 3.3 V, 2.4 V, 1.8 V, and, more recently, 1 V and even 0.9 V analog supplies in deep nanometer CMOS data converters as 40 nm or 28 nm. This has inevitably led to formidable design challenges due to lowering voltage headroom and the ability to design analog circuits with a sufficiently low noise power spectral density with rapidly shrinking usable signal power.

The greater adoption of CMOS processes for high-performance data converters for wireless infrastructure has also fueled another trend. Scaled CMOS processes have enabled dramatic improvements in terms of both cost- and power-effective digital signal processing functionality. Therefore it is very common in present-day wireless infrastructure data converters that a good deal of the digital post-processing in the receive path is integrated on the same die with the ADC and, conversely, that the digital pre-processing in the transmit path is integrated on the same die with the DAC. Such digital functions include, for example, digital down conversion, filtering, channel separation in the case of the receive path; and consist, for example, of digital up conversion, interpolation, filtering, etc., in the case of the transmit path.

Furthermore, this on-chip availability of efficient digital functionality has also enabled the practical implementation of on-chip calibration and nonlinear correction schemes for some of the cited analog-domain shortcomings. So, in a way, the source of some of the analog design grief introduced by nanometer processes can also be tackled by means of the rich digital processing power introduced by Moore’s law by a broad new slew of techniques loosely categorized as “digitally assisted analog (and RF) design.”

Furthermore, the increasing demand for larger data throughput, combined with the increasing availability of computational DSP power fueled by Moore’s law, has driven the demand from BTS manufacturers for wider and wider bandwidth signal chains able to process co-existing and different communication standards (not only GSM channels, but also LTE, WCDMA, etc.). Without doubt, that has made the RF front-end and the data converters the “performance bottleneck” of this class of radio systems. Along with that, the power, functionality, and cost advantages of DSPs have fueled the quest for the “holy grail” of radios, known as “software radio” and consisting of a signal chain where the RF and analog front-end are increasingly smaller and where the analog-to-digital conversion and the digital-to-analog conversion boundaries move closer and closer to the antenna, allowing more of the (de-)modulation/filtering/processing of the communication channels to be efficiently and reliably performed in the digital domain. Indeed one of the chief challenges of this quest lies in the fact that moving the boundary between the physical analog medium and the digital one toward higher frequency or wider bandwidth is paid for by dramatic increases in power consumption to perform the conversion.

It is mainly because of this reason that for a given set of communication specifications and development and implementation costs a balanced choice for the borderline between analog and digital leads to sensitive signal-chain trade-offs.
In many commercial cell phone BTSs this boundary lies presently between the tens and hundreds of MHz and where the ADC samples the lowest intermediate frequency (IF) stage of a heterodyne scheme or where the DAC directly synthesizes the signals at one of the IF frequencies, or possibly at RF.

Another critical design challenge originates from the need, mentioned above, to develop a BTS that is physically small in size: going from a unit similar in size to a small refrigerator to one similar to a desktop PC or possibly slightly bigger than a laptop. To reduce physical size, higher integration is certainly one lever, but most importantly heat removal is a very important challenge. Heating sinks, fans, and other sizeable devices for heat removal and management need to be eliminated. That means the electronics need to dissipate less heat and need to be able to operate in a much hotter ambient temperature. Clearly the previously cited power consumption challenge originating from increasing communication performance demands is further aggravated by these much more challenging operating environment conditions. Not only circuit design technology and silicon reliability are challenged. Electrical, thermal, and mechanical aspects of package technology, assembly and manufacturing, printed circuit boards, to cite a few, come into play and trade-offs between all these aspects take center stage in the design development process.

1.4 This book

This book aims to provide an overview of the main and most current technical topics in radio-frequency and analog/mixed-signal IC design for wireless infrastructure. The chapters are contributed by some of the most well-respected professionals in this field both from industry as well as academia.

The chapter authored by H. Darabi provides a broad overview of the architectures and system trade-offs involved in the overall design of CMOS transceivers. Following that, the individual chapters dive into covering the challenges and the design techniques associated with all the main functional blocks in modern commercial cellular base station systems. Following an order that somewhat mirrors the cascade of stages between the antenna and the DSP, we begin with a chapter on the design of low-noise, high-linearity amplifiers (LNAs) authored by D. Leenaerts as well as another chapter on RF power amplifiers written by M. Acar et al.

That is followed by a chapter on frequency synthesizers/PLLs contributed by S. Levantino and C. Samori describing low phase noise oscillators used in down and up conversion. And, of course, coupled with that is a chapter on mixers and modulators by W. Redman-White. The special case of low noise down-converters for satellite communication systems is covered in a chapter by P. Philippe et al. The latter concludes the part of this book on what is commonly considered as the true radio-frequency electronics of this class of infrastructure radios.

The many classes of analog-to-digital and digital-to-analog converters found in base stations are discussed in the chapters that follow. R. Schreier and H. Shibata authored a chapter on emerging continuous time band-pass ΔΣ ADCs for communication
applications. A more established ADC architecture in this arena is the pipelined ADC. That is the topic of the following chapter by M. Elliott and B. Murmann. Another ADC architecture that is gradually emerging as a viable option is the SAR ADC. Interleaving multiple lower-sampling-rate ADCs allows the building of overall higher-sampling frequency converters as described in the chapter by K. Doris et al. that follows.

Finally a chapter by G. Engel and G. Manganaro describes the other side of converters, namely modern high-performance digital-to-analog converters for the transmit path.

Last but not least, the chapter on time-to-digital conversion for digital frequency synthesizers describes an emerging breakthrough alternative to some of the other approaches in frequency synthesis as well as domain conversion. This chapter is authored by M. Perrott and concludes the volume.

**CONCLUSIVE REMARKS**

Concluding this introduction, the two editors of this volume would like to acknowledge and thank the many authors of this book, who, on rather short notice and on a fast-paced schedule, have graciously managed to contribute a comprehensive and cohesive set of outstanding chapters on very critical topics for a very rapidly evolving and highly competitive space. Given the fast pace of innovation and the breadth of this field there is no doubt that reading this material will both answer questions and trigger new ones. In fact, the contents are very much on the tipping point of today’s state-of-the-art and knowing what the right questions and the challenges are is as important as being able to tackle them.

The editors would also like to thank the anonymous reviewers. Providing us with their constructive criticism and suggestions has allowed us to improve the organization and blend of the topics, hence helping us to structure the many moving parts of this volume into a more organic and thorough treatise of the topic.

Our thanks also go to the staff at Elsevier and, in particular, to the senior commissioning editor Tim Pitts. Tim, with his British gentleman style, his instinctive flair, and his punctual prodding, was able to first convince us to embark on this adventure and then to actually deliver it on a schedule that is sensitive to the timeliness of its contents.

Last but not least, we thank our families for their unconditional support and encouragements, despite the precious time taken away from them after coming back from already long and tiring days at our regular day jobs.
2.2 3/4G transceiver architecture design

The 3G standard as introduced initially in 2001 [4] is a spread-spectrum wideband CDMA system using a QPSK modulation scheme and supports up to 19 bands, the most widely used ones are band I (2110–2170 MHz for downlink, 1920–1980 MHz for uplink) and bands II, III, VIII, and V which are identical to the four GSM/EDGE bands shown in Table 2.1 (PCS, DCS, GSM 900, and GSM 850, respectively). Several other bands such as bands IV, VI, or IX are a subset of the aforementioned five bands, while the less commonly used band VII uses a more challenging higher frequency (2620–2690 MHz for downlink, 2500–2570 MHz for uplink). The channel spacing is 5 MHz, while the signal itself is about ±1.92 MHz wide. The TX-RX separation ranges from 30 MHz for lowbands (although most commonly used lowbands are 45 MHz) and up to 190 MHz for band I. The recent drive for higher data rates has, however, introduced several additions to the original 3G, such as HSPA, which uses 16-QAM in RX mode, and HSPA+, which supports 64-QAM, and can achieve data rates of up to 21 Mbps.

Unlike GSM/EDGE, 3G is an FDD (frequency division duplexing) system. The full-duplex nature of the system, that is, the simultaneous operation of the RX and TX causes several challenges unique to 3G, although the spread spectrum nature of it [19–22] relaxes some of the blocking requirements. Ideally, an external duplexer realized by two highly selective filters separates the receive and transmit signals (Figure 2.15), but in practice, due to the finite isolation of the duplexer, some of the strong TX signals leak to the RX input, causing two issues: First, the TX noise falling in the RX band effectively degrades the receive noise figure. Second, when mixed by a large out-of-band blocker (for example, the blocker at half-duplex frequency) due to the front-end third-order nonlinearity, the RX is desensitized. To overcome these issues, external filters are traditionally placed at the TX and RX ports to suppress the TX noise and leakage, thus relaxing the phase noise and linearity requirements of the transceiver. In the case of the transmitter output, the SAW filter relaxes the noise requirement of the TX chain by providing some filtering, whereas the receiver SAW filter attenuates the TX residual leakage and any other blocker, thereby relaxing the linearity requirements of the RX chain. However, most modern 3G designs are SAW-less, which demands more stringent phase noise (for both RX and TX) and linearity (for RX). In this section we will look into some of these requirements in more detail.

2.2.1 3G receiver requirements

Most recent 3G receivers usually adopt a zero-IF architecture shown in Figure 2.2 [19–22]. As the received signal is wide compared to 2G, common issues such as 1/f noise and DC offset are less problematic, thus justifying a zero-IF design due to its simplicity and low power consumption. On the other hand, the wideband 3G signal would require a large IF (a few MHz) if one were to use a low-IF scheme, which translates to higher power consumption for the ADC and IF analog blocks, without
gaining much performance. The receiver is SAW-less; however, it benefits from the filtering provided by the duplexer, which is similar to a 2G SAW filter for a given band. Therefore the out-of-band blockers (except for the TX leakage and related blockers) are generally not a major concern.

### 2.2.1 Sensitivity

The receiver noise figure is calculated based on a reference sensitivity requirement of $-117$ dBm/3.84 MHz (for band I as an example), and for a 12.2 kbps reference measurement, with a spreading factor of 128 (or 21 dB) as shown in Figure 2.16.

The spreading factor (SF) is the ratio of the chip rate, 3.84 MHz, to the actual data rate, which is 30 kbps in this measurement. In general, depending on the physical conditions of the link and the quality of the reception, the spreading factor ranges from 4 to 512, where the SF of 4 corresponds to the highest throughput but requires a stronger signal. Since the QPSK requires a modem SNR of 7 dB, with 4 dB of coding gain and 21 dB of spreading factor, the effective SNR is $7 - 4 - 21 = -18$ dB. Thus the NF is $174 - 117 + 18 - 10 \times \log(3.84\text{ MHz}) = 9.2$ dB. Unlike the 2G receiver where the sensitivity is merely set by the receiver thermal noise, the NF here is derived by several other factors as well, such as the TX noise in the RX band, the receiver second-order non-linearity, and the reciprocal mixing. We will discuss the impact of TX noise in the next section (Eq. (2.5)). The receiver second-order non-linearity effectively amplitude de-modulates the TX leakage, which results in a wide signal spread at twice the desirable signal bandwidth at DC, as shown in Figure 2.17.

**FIGURE 2.16**

3G RX noise figure.

**FIGURE 2.17**

TX leakage causing second-order nonlinearity concerns.
Similar to our IIP2 analysis for the 2G receivers, the required IIP2 for the 3G RX can be calculated for a given TX leakage. Assuming a duplexer isolation of 45 dB in the transmit frequency, and 4 dB loss for the duplexer/switch, the TX leakage is $24 + 4 - 45 = -17$ dBm at the LNA input, assuming a full transmit power of 24 dBm at the antenna. As $IIP2 = 2 \times P_B - \text{Sensitivity} + \text{SNR}$, with $P_B = -17$ dBm, an IIP2 of $(2 \times -17 - 13) + 117 - 18 = +52$ dBm will cause a sensitivity of $-117$ dBm. The 13 dB is a constant found through simulations to consider the spreading on the TX envelope squared (Figure 2.18). Depending on the duplexer, most 3G receivers target an IIP2 of better than $+45$ dBm specified at the duplex frequency (190 MHz away for band I for instance). With a SAW filter placed after LNA however, the TX leakage is attenuated substantially and the IIP2 is relaxed accordingly. Similarly a phase noise of PN at the duplex frequency on the RX VCO/LO defines a thermal noise figure of $174 + P_{TX} + \text{PN}$, where $P_{TX}$ is the TX leakage. Now a phase noise of $-155$ dBc/Hz at the duplexer frequency alone results in a noise figure of 2 dB, which adds to the overall budget. Unlike the case of 2G, where the sensitivity is relaxed by 3 dB in the presence of the blockers, here the mentioned impacts all add up in the extreme case.

Now assuming 3 dB insertion loss for the duplexer, 1 dB loss for the switch, and another 1 dB degradation due to the impacts of second-order nonlinearity, TX noise, and reciprocal mixing, then the thermal receiver noise figure is 4.2 dB at worst case. With 1.5 dB margin for PVT, the receiver typical thermal noise figure is about 2.5 dB, very similar to the GSM. Note that one may trade the receiver thermal noise for a more stringent IIP2 or phase noise, for example, or perhaps a better (more expensive) duplexer with higher isolation.

The impact of blockers is generally less important than GSM, except for the cases driven by the TX leakage such as duplex IIP2, which was discussed previously. Another example is shown in Figure 2.18 as follows.

A blocker at half-duplex frequency mixed with the TX leakage results in an IM3 signal down-converted on top of the desirable signal at baseband due to the third-order nonlinearity of RX front-end. The sensitivity is allowed to be relaxed by 3 dB in the out-of-band blocker scenarios, and the IIP3 is calculated as follows: $2 \times IIP3 = P_{TX} + 2 \times P_B - \text{Sensitivity} + \text{SNR}$. The TX leakage was found to be $-17$ dBm for 45 dB of isolation, and assuming 30 dB of filtering due to the duplexer and $-15$ dBm blocker power as specified by 3GPP standard, IIP3 is found to be
\((-17 - 2 \times 45 + 114 - 18)/2 = -5.5\text{dBm}\). With PVT and production margins, and some room left for other factors such as phase noise or second-order nonlinearity as discussed before, the half-duplex IIP3 is typically specified to be close to 0 dBm, which is much more challenging than what is needed for GSM/EDGE \((-13\text{dBm at } 3\text{MHz})\). Again a filter placed between the LNA and mixers would help at the expense of size and cost. Alternatively one may choose either integrated LC notch filtering [21], or use high-Q n-path filtering [14–15] shown in Figure 2.20 [17]. In the front-end of Figure 2.19, the LNA is replaced by a low-noise transconductor, driving current-mode passive mixers. Due to reciprocity, the passive mixers up-convert the low-pass baseband impedance to RF providing high-Q selectivity on the LNA output, thus suppressing the TX leakage. With this prototype IIP3 of better than 0 dBm with 2.5 dB noise figure is achieved.

The maximum input level is \(-25\text{dBm}\) for it is typically easily met through gain control in the receiver.

### 2.2.1.2 Blocking requirements

3GPP specifies an adjacent channel (at +5 or \(-5\text{MHz away}\)) selectivity (ACS) of 33 dB specified for two cases of desired signal at 14 or 41 dB above the reference sensitivity. Since desirable signal is relatively strong, typically noise is not a factor and,

**FIGURE 2.19**
An example of a 3G RX front-end.
CHAPTER 3 Low-Noise Amplifiers for Cellular Wireless Infrastructure

3.3.1 Single-stage BiCMOS LNA

A bipolar single-stage cascode topology, also referred to as a common-emitter (CE), common-base (CB) topology, is shown in Figure 3.5. Transistor Q₁ is configured as the common-emitter device, and Q₂ as the common-base device. The LNA is inductively loaded by L₁ and to have simultaneous power and noise matching towards the source impedance inductive degeneration by means of Lₑ has been applied. In fact this is a similar technique used in the GaAs LNA of Figure 3.2. Additionally feedback capacitor Cₑfb is added to improve the power matching at the input. Both bipolar transistors are resistively biased (R₁ and R₂).

A cascode topology can easily provide more than 15 dB gain, but has the drawback that the output impedance is rather high, making matching to a 50Ω load difficult.

### Table 3.2 Comparison of Two Different 0.25 μm SiGe:C BiCMOS Processes from NXP. LV Reflects a High-Performance Low-Voltage Device, HV Refers to the High-Voltage Device

<table>
<thead>
<tr>
<th>Parameter</th>
<th>QuBIC4X</th>
<th>QuBIC4Xi</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LV NPN</td>
<td>HV NPN</td>
</tr>
<tr>
<td>β</td>
<td>400</td>
<td>320</td>
</tr>
<tr>
<td>fT</td>
<td>130</td>
<td>60</td>
</tr>
<tr>
<td>fmax</td>
<td>180</td>
<td>120</td>
</tr>
<tr>
<td>NFmin@2GHz</td>
<td>0.60</td>
<td>–</td>
</tr>
<tr>
<td>BVCEO</td>
<td>1.8</td>
<td>3.3</td>
</tr>
<tr>
<td>BVCEO</td>
<td>6</td>
<td>13</td>
</tr>
</tbody>
</table>

FIGURE 3.4
Cut-off frequency (black) and fNFmin0.7dB (gray) as a function of the collector-emitter current. Emitter area of the NPN device is 1.2 μm².

3.3.1 Single-stage BiCMOS LNA
To overcome this problem, an impedance transformation can be implemented by means of a center tap on load inductor $L_1$.

In this specific example, a bypass mode has been implemented. In this mode ("By" becomes "high"), the LNA is turned off and the input signal at $RF_{in}$ is routed via $M_1$ towards output $RF_{out}$. Inductor $L_3$ is used in bypass mode to tune out the base-emitter capacitance of $Q_1$, seen through $M_1$ and which is then unbiased. Inductor $L_3$ will also contribute to the output matching in active mode, together with $C_2$.

As in bypass mode the overall linearity of the LNA can be disturbed by $M_1$, the influence of the nonlinear device capacitances, i.e. drain-to-bulk and source-to-bulk capacitances, need to be reduced. This can be realized by surrounding the device by deep-trench isolation (DTI) and by connecting the bulk silicon outside this DTI region to ground. A very high resistive path from the back gate of $M_1$ to ground can be realized in this way. In fact, thanks to the DTI, the local substrate emulates the substrate of an SOI technology.

This topology has been used to realize an LNA for a $1.95\,\text{GHz}$ WCDMA base station application [15].

The LNA has been realized in the $0.25\,\mu\text{m}$ SiGe:C BiCMOS technology of NXP (QuBIC4Xi). The die photo is shown in Figure 3.5 (right). For ease of understanding the most important passive components are indicated on the die photo. The measured NF at room temperature for the cascode LNA is given in Figure 3.6, indicating an NF of $0.6\,\text{dB}$ at $2\,\text{GHz}$. The power consumption is $290\,\text{mW}$ from a $5\,\text{V}$ supply in active mode. Other measured performances are provided in Table 3.3, indicating that this BiCMOS design can compete with single-device GaAs-based LNA as discussed in the previous section.

**FIGURE 3.5**
Circuit diagram for a cascode-topology (left, biasing circuitry not shown) and the die photograph (right).
INTRODUCTION

Wireless communication is an indispensable part of our daily life in today’s world. Use of smartphones, tablet PCs, and other wireless devices/services creates a huge amount of data traffic. With the increasing number of subscribers, expected to be more than 6 billion by 2014 [1], handling high data traffic with limited frequency resources will continue to be one of the prime challenges for wireless communication industries. Transmission of huge amounts of data implies high energy consumption. The global information communication technology (ICT) industry accounts for about 2% of the total human CO2 footprint, which is comparable to the air traffic CO2 emissions all around the world [2]. Of the 2% total ICT emission, 25–30% is produced by worldwide telecom infrastructures and devices [3]. Therefore, energy consumption due to telecom infrastructures is significant. Besides, most of the energy in mobile networks is consumed by the base stations [4,5]. Typically more than half of the energy consumption in a base station is due to the RF power amplifier, as can be seen in Figure 4.1. Therefore, improving the efficiency of the power amplifier will decrease the energy consumption and hence reduce the cost of telecom infrastructures.

Increasing the efficiency of the power amplifiers in base stations is very challenging for many reasons. A typical property of the signals in third-generation (3G) and beyond communication systems is high peak-to-average power ratio (e.g. in wideband code division multiple access (WCDMA) typically 10 dB), requiring high linearity of the transmitting amplifier. Consequently, PAs are typically dimensioned for the peak power condition, but are operated most of the time at significantly lower power levels (i.e. power back-off). As a result, even when using a high-efficiency amplifier class, e.g. (inv.) class B [6], class E [7] or (inv.) class F [8], the peak efficiency might be high, but the average amplifier efficiency can be rather low. For this reason, there is a renewed interest in highly efficient PA architectures at back-off power levels that were introduced in the 1950s and 1960s.

Figure 4.2 shows the power amplifier concept evolution in wireless communication systems. The design of power amplifiers in early 2000 was based on linear but
low-efficiency power amplifier topologies such as class A and class AB. Later, use of digital pre-distortion techniques and Doherty power amplifier topology (DPA) has helped to increase efficiency. Further demand for high-efficiency in wireless transmitters requires a shift of the PA topology to digital transmitters, switch-mode power amplifiers (SMPA) such as linear amplification using nonlinear components (LINC) or envelope elimination and restoration (EER).

Most of today’s base station PAs use LDMOS technology. Higher RF performance of GaN over LDMOS (e.g. higher supply voltage, higher input/output impedance, etc.) will make it the preferred transistor technology for future base station PAs.

In this chapter, Section 4.1 explains the basics of Doherty PAs by presenting a wideband implementation. Afterwards, an outphasing switch-mode PA will be introduced in Section 4.2. Finally, an essential part of switch-mode power amplifiers, drivers, will be presented in Section 4.3.
4.1 Wideband Doherty Power Amplifier

Currently, the Doherty power amplifier (DPA) [9] represents the most commonly used high efficiency concept in base station applications. Its popularity results from its high-efficiency performance achieved at a low hardware complexity and cost level [10,11]. However, a well-known disadvantage of the DPA is its narrow bandwidth (typically ≤10%) [12,13], which complicates its application in multi-band/multi-standard communication systems. Consequently, custom DPA solutions for each individual need in the market have to be developed, raising costs and yielding logistic problems.

To address this limitation, we investigate how the DPA bandwidth for high-efficiency operation can be expanded. This chapter is organized as follows: after providing a brief introduction to the Doherty power amplifier, we first discuss the DPA bandwidth restrictions in Section 4.1.1. In Section 4.1.1 we evaluate various matching topologies (mainly addressing the wideband compensation of the output capacitance of these devices), connection schemes, and Doherty power combiners that extend the DPA bandwidth. The actual circuit realizations are given in Section 4.1.2, followed by experimental verification in Section 4.1.3.

4.1.1 Theory of Doherty power amplifiers

Doherty power amplifier operation is a well-established technique to increase the average efficiency of microwave amplifiers [14]. In this technique the RF amplification is accomplished by using multiple branch amplifiers in parallel. When the power outputs of these branch amplifiers are cleverly combined, active load modulation occurs, which helps to improve the average efficiency of the overall DPA amplifier. Currently, there exist various Doherty power amplifier implementations, e.g. the symmetrical two-way DPA [15], the asymmetrical two-way DPA [11], and the three-way DPA [12]. However, in the following sections only the bandwidth performance of the two-way DPA is discussed in detail for reasons of simplicity. The results obtained from this analysis can be easily extended to cover other more complex DPA architectures. The diagram of a two-way Doherty power amplifier (DPA) in its most elementary form is given in Figure 4.3. Here the main and peak...
simple multiplexers implement the correlators. This results in reduced silicon area and power consumption.

The test chip in Figure 5.18 implements in 65 nm CMOS a digital $\Delta \Sigma$ fractional-$N$ PLL [18] with a narrow-range TDC and with the so-far-discussed scheme for the correction of DTC nonlinearity. Measurements confirm that this approach is effective in reducing the in-band fractional spurs induced by DTC nonlinearity from $-44$ to below $-68$ dBc. The measured spectra obtained for a near-integer channel, gradually enabling the spur-correction algorithms are shown in Figure 5.19: (a) no correction, (b) cancelation of $\Delta \Sigma$ quantization error, (c) TDC element randomization, (d) DTC nonlinearity correction. The combination of these techniques demonstrates a reduction of all spurs below $-57$ dBc.

### 5.3.3 Fractional-$N$ digital PLLs with single-bit TDCs

Following the argument discussed in the previous subsections, the deleterious effect of TDC mismatches and systematic errors on fractional spur generation could be in principle removed by adopting a single-bit TDC. A single-bit TDC, which can be implemented in practice as a D-type flip-flop, detects whether the flip-flop D input leads or lags the clock input. In practice, it acts as a hard limiter on the time delay between its two inputs. For this reason, in the field of control theory, this detector is often referred to as *lead–lag detector* or *bang-bang detector*. Given its very simple implementation, the additional advantage of a single-bit TDC over a multi-bit one is obviously the reduction of the synthesizer power consumption, especially considering that the TDC is typically one of the most power-hungry blocks in a digital PLL.

Although widely used in PLLs designed for clock-and-data-recovery applications, thanks to its high speed, this kind of detector is rarely used in the field of frequency synthesizers. Except for the case of integer-$N$ frequency synthesis (where bang-bang detectors have recently been employed both in analog and digital implementations,

![FIGURE 5.18](Image)

Die photograph of the digital PLL with narrow-range TDC in [18].
A nonlinear phase detector is typically avoided. The main reason is that in fractional-\(N\) PLLs, the \(\Delta \Sigma\) dithering of the divider modulus produces high-frequency quantization noise, which is supposed to be filtered out by the loop filter. A highly nonlinear block in the loop such as a bang-bang phase detector produces spectrum folding of this quantization noise and it results in much higher PLL in-band noise.

A possible solution to the nonlinearity of the single-bit TDC consists of closing it in a loop with the \(\Delta \Sigma\) modulator [43]. The resulting circuit is the Copeland’s frequency discriminator. Since this circuit acts as a frequency detector, the resulting PLL is a type-I, which intrinsically offers poorer phase noise performance. An alternative approach providing noise shaping of the quantization noise of the single-bit TDC can be found in [44].

The issue of dithering could in principle be solved by adopting a DTC-based fractional-\(N\) divider similarly to the previously discussed case of the low-range TDC. However, since the residual dithering of the PLL time error is as large as the DTC time resolution, the TDC range in the previous case was designed to be greater than or
clocked at 4 GHz, the ADC consumes 550 mW in the two LC modes and 750 mW in the active-RC mode.

8.3.1 NTF and STF

Figures 8.26, 8.27, and 8.28 show measured output spectra and STFs for \( F_0 = 1 \) GHz, 450 MHz, and 0 MHz, demonstrating wide center-frequency tunability from 0 to \( F_S/4 \) with no STF peaking. The STF roll-off at low frequencies in the \( F_0 = 0 \) MHz case is due to an off-chip balun and off-chip AC-coupling capacitors. For the preceding values of \( F_0 \), dynamic range and peak SNR are 67/79/73 dB and 63/72/71 dB, respectively.

The noise spectral density (NSD) of the ADC depends on the BW setting because the back-end noise degrades the NSD at the inband edges in wide-band configurations. The ADC achieves a mean noise density of -159/-156/-152 dBFS/Hz for BW of 50/100/150 MHz at \( F_0 = 400 \) MHz as shown in Figure 8.29. Beyond \( BW = 150 \) MHz, the increase in NSD at the band edge is too great to be of practical value.

By setting the BW to the impractical value of 300 MHz, however, the notches of the NTF become clearly visible, which allows the resonator, \( Q \), to be determined. Figure 8.30 shows that the \( Q \) of the active-RC resonators is high enough that the notch width is less than 25 MHz. Thus the resonator \( Q \) is high enough to prevent degraded noise shaping as long as the BW is more than 25 MHz. Another factor which limits the achievable noise shaping is the frequency accuracy of the NTF zeros. This design
FIGURE 8.26
Measured single-tone output spectrum at $F_0 = 1$ GHz and $BW = 75$ MHz. Dashed and solid lines represent STF and output spectra.

FIGURE 8.27
Measured single-tone output spectrum at $F_0 = 450$ MHz and $BW = 100$ MHz. Dashed and solid lines represent STF and output spectra.
uses a combination of N-poly (positive temperature coefficient) and P-poly (negative temperature coefficient) resistors to reduce the temperature-dependence of the resistors. Temperature sweeps confirm that the NTF zeros shift by less than 1% over the $-40–125^\circ$C range.

In theory, the alias attenuation afforded by this feedback ADC exceeds 130 dB. In practice, feed-through in the integrators and other leakage paths reduce the

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>dBFS/NBW, dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-100</td>
</tr>
<tr>
<td>100</td>
<td>-50</td>
</tr>
<tr>
<td>200</td>
<td>0</td>
</tr>
<tr>
<td>300</td>
<td>50</td>
</tr>
<tr>
<td>400</td>
<td>100</td>
</tr>
</tbody>
</table>

**FIGURE 8.28**
Measured single-tone output spectrum at $F_0=0$ MHz and $BW=150$ MHz. Dashed and solid lines represent STF and output spectra.

NSD at various $BW$; $F_0=400$ MHz, $F_S=4$ GHz.

**FIGURE 8.29**